

CHAPTER 4

CRYSTALLINE SILICON SOLAR CELLS

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“Vast Power of the Sun Is Tapped by Battery Using Sand Ingredient.”
Front page headline, New York Times, 26 April 1954.

4.1 Overview

Front page headlines in the New York Times and the Wall Street Journal in 1954 heralded to the world the demonstration of the first reasonably efficient solar cells, an event made possible by the rapid development of crystalline silicon technology for miniaturised electronics. Since that time, the majority of solar cells fabricated to date have been based on silicon in monocrystalline or large-grained polycrystalline form. There are two main reasons for this. One is that silicon is an elemental semiconductor with good stability and a well-balanced set of electronic, physical and chemical properties, the same set of strengths that have made silicon the preferred material for microelectronics. The second reason why silicon cells have been so dominant is that the success of silicon in microelectronics has created an enormous industry where the economies of scale directly benefit the presently smaller photovoltaics industry.

Most silicon cells have been fabricated using thin wafers cut from large cylindrical monocrystalline ingots prepared by the exacting Czochralski (CZ) crystal growth process and doped to about one part per million with boron during ingot growth. A smaller but significant number use what are referred to as ‘multicrystalline’ wafers sliced from ingots prepared by a simpler casting (or, more generally, directional solidification) technique, which produces large-grained polycrystalline ingots. To produce a cell, these boron-doped starting wafers generally have phosphorus diffused at high temperatures a fraction of a micron into the surface to form the p - n junction required. Metal contacts to both the n - and the p -type side of the junction are formed by screen printing a metal paste that is then densified by firing at high temperature. Each cell is typically 10–15 cm either in diameter or along either side if square or rectangular.

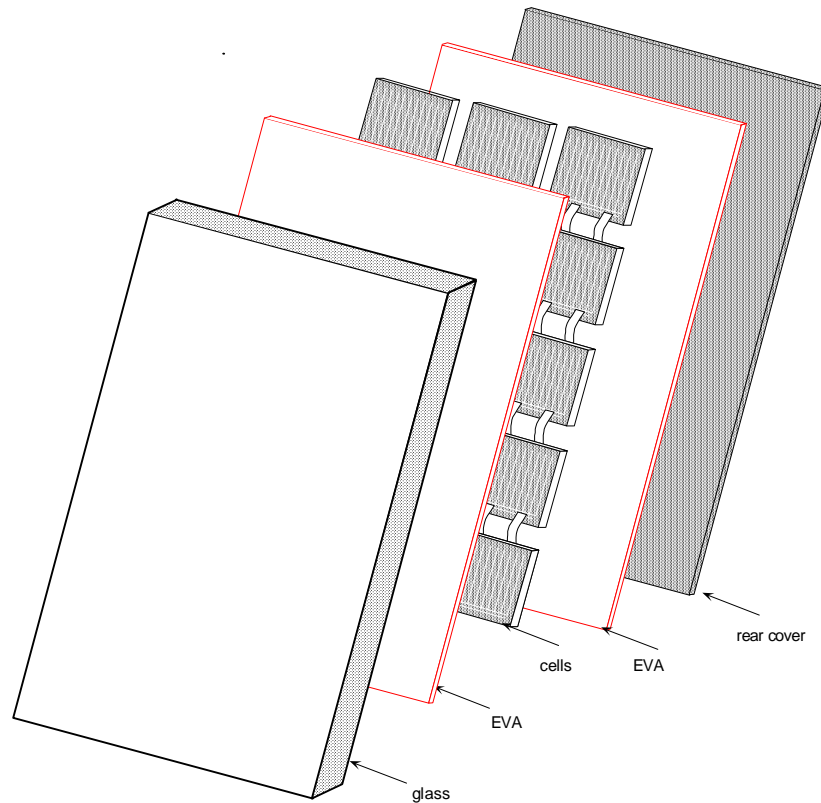


Figure 4.1 Exploded view of a standard silicon photovoltaic module. The different layers shown are laminated together under pressure at a temperature around 140–150 C where the transparent EVA (ethylene vinyl acetate) softens and binds the different layers together on cooling. Source: Green and Hansen (1998).

Cells generally are sold interconnected and packaged into a weatherproof, glass-faced package known as a module, as shown in an exploded view in Fig. 4.1. Each module typically contains 36 cells soldered together in series. Since each individual cell gives a maximum output of about 0.6 V in sunlight, this results in a module of over 20 V maximum output voltage, sufficient for fully charging a normal 12 V lead-acid battery. The output current of each cell depends on its size and the sunlight intensity (solar irradiance) but generally would lie in the 2–5 A range in bright sunshine. The packaging consists of a glass/polymer laminate with the positive and negative leads from the series-connected cells brought out in a junction box attached

to the module rear. Such modules have proved extremely reliable in the field with all manufacturers offering a 10–25 year warranty on the module power output, one of the longest warranties on any commercial product (saucepans have been suggested as one of the few manufactured products with a comparable warranty period!).

The efficiency of the cells in the module would typically lie in the 12–16% range, less than half the fundamental ‘detailed-balance’ limit of 33% for silicon (Tiedje *et al.*, 1984). Module efficiency is slightly lower than that of the constituent cells due to the area lost by frames and gaps between cells, with module efficiency generally lying in the 10–13% range. Over the last few years, commercial cells and modules of significantly higher performance have been available in multi-megawatt quantities using a more advanced cell processing technology (developed by the author’s research group), discussed in more detail in the text. This technology produces cells of 17–18% efficiency and module efficiency in the 14–15% range. (Unless otherwise noted, all efficiencies quoted in this chapter are at standard test conditions, namely with a cell temperature of 25 C under 1000 W m⁻² sunlight intensity with the standard global air mass 1.5 spectral distribution).

This chapter discusses the historical and ongoing links between silicon solar cells and the broader microelectronics industry. Also discussed are standard and improved methods for preparing silicon cell substrates and for processing cells to extract as much performance as possible from such substrates at the lowest possible overall cost. The chapter also describes recent progress with supported silicon films. These provide a ‘thin-film’ approach for transforming silicon technology from the thoroughbred of the twentieth century to a much lower cost, market-leveraging workhorse of the twenty-first.

4.2 Silicon cell development

The development of silicon photovoltaics is inextricably intertwined with the development of the general silicon electronics field and the subsequent founding of the microelectronics industry. The rapid increase in interest in the properties of doped silicon in the 1940s was triggered by the astonishing photovoltaic properties demonstrated by serendipitously formed *p-n* junctions, as described below. This increased interest led directly to the development of point contact and junction transistors and ultimately to integrated circuits.

The earliest commercial silicon electronic devices were silicon point-contact or “cat’s whisker” diodes which date from the early 1900s (Riordan and Hoddeson, 1997). These devices rectified electrical signals at a junction formed by pressing a thin

metal wire against a piece of polycrystalline silicon (other semiconductors, such as silicon carbide, were also used). These cat's whisker diodes were key components in early radios. By the 1930s, thermionic valves had replaced these diodes in most applications. However, the evolving field of microwave technology created a renewed interest in the cat's whisker diodes in the mid-1930s. At Bell Laboratories in the USA, Russell Ohl guessed that impurities were the cause of the erratic behaviour often observed whereby the cat's whisker only operated correctly if located on a 'hot spot' in the silicon. Ohl therefore encouraged colleagues to grow samples of purer silicon, by melting the purest material available in a quartz capsule, and then cooling. In one specific ingot, the eighteenth in the series (Riordan and Hodgeson, 1997) which had been prepared by very slow cooling, Ohl and his colleagues found unusual properties, including a surprisingly large photovoltage of about half a volt when the ingot was illuminated by a flashlight. The silicon in this ingot showed two distinct types of properties, dubbed "positive" (*p*-type) and "negative" (*n*-type), depending on the polarity required for easy current flow between the material and a metal wire placed on the silicon surface, and also the polarity of voltage observed under illumination. It was quickly realised that the junction between the *p*-type and *n*-type regions, the *p-n* junction, was responsible for the unusual properties of the original ingot. The first silicon solar cells were formed by cutting the ingot to include sections with both a *p*- and *n*-type region and applying metal contacts (Ohl, 1941). These earliest silicon solar cells, shown in Fig. 4.2a, appear, based on available data, to have been only a fraction of percent efficient, but were still very much better in performance than earlier photovoltaic devices which had been based on selenium or cuprous oxide.

The "grown-in" junctions in the earliest cells arose from the serendipitous distribution of *p*-type (boron) and *n*-type (phosphorus) impurities in the silicon resulting from the slow solidification process. Ohl realised that more controllable ways of forming the junction would be likely to give better performance. In the early 1950s, he was involved in experiments aimed at forming surface junctions by implanting helium at high energy into the surfaces of *p*-type polycrystalline silicon (Kingsbury and Ohl, 1952). Although this approach produced improved cells of efficiency estimated to be up to 1%, (Fig. 4.2b), this work was soon overtaken by independent improvements in silicon technology also made at Bell Laboratories, particularly in two areas. The first was the development of techniques for preparing single crystals of silicon using the Czochralski method. The second was the formation of junctions by the high-temperature diffusion of dopant impurities into the silicon surface. Combining these two techniques, researchers at Bell Laboratories were able to announce the first modern silicon solar cell in early 1954, in one of the early successes of the diffused junction approach (Chapin *et al.*, 1954). Figure 4.2c shows the resulting cell structure.

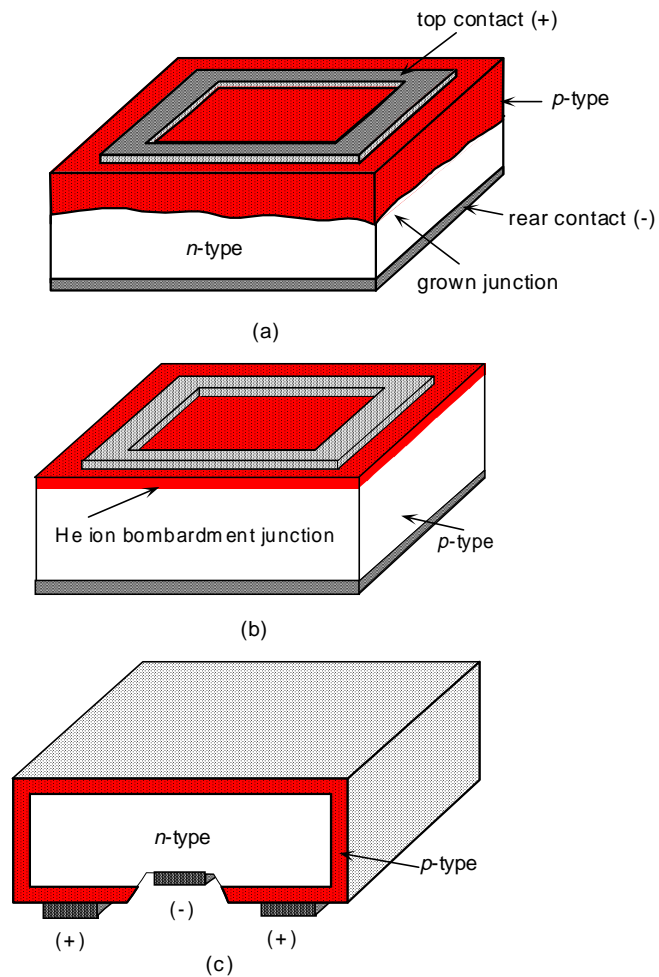


Figure 4.2 (a) Silicon solar cell reported in 1941 relying on 'grown-in' junctions formed by impurity segregation in recrystallised silicon melts; (b) helium-ion bombarded junction device of 1952; (c) first modern silicon cell, reported in 1954, fabricated on single-crystalline silicon wafers with the *p-n* junction formed by dopant diffusion. Source: Green (1995).

The impressive performance of these cells by previous standards, up to 6% energy conversion efficiency, created enormous interest at the time, as the newspaper headline at the beginning of this chapter suggests, and it also generated unbounded enthusiasm for the future of these devices. This enthusiasm proved to be premature, although the cells did find an almost immediate application in spacecraft. Space applications drove the rapid improvement in cell technology such that, by the early 1960s, cell energy conversion efficiency of about 15% under terrestrial sunlight had been demonstrated and cells had found a secure market niche in providing power for a rapidly increasing number of satellites (Wolf, 1976). The basic cell design which evolved (Fig. 4.3a), remained unchanged from the early 1960s for almost a decade. In the early 1970s, a reassessment of cell design at COMSAT Laboratories showed that a shallower diffusion combined with more closely spaced metal fingers could give a substantial improvement in the cell performance by improving the response to blue wavelengths (Lindmayer and Allison, 1973). The resulting cells, shown in Fig. 4.3b, known as “violet” cells due to their characteristic colour arising from the shorter wavelengths reflected, produced the first improvement in cell performance for over a decade. This improvement was augmented by the realisation that incorporating a thin heavily doped layer under the back contact, a so-called “back-surface field”, gave unexpected benefits (Godlewski *et al.*, 1973). This approach worked best if the rear doped layer was formed by alloying the underlying silicon with aluminium deposited over the rear of the cell. Not long afterwards, the idea of using anisotropic chemical etches to form geometrical features on the silicon surface was successfully demonstrated, also at COMSAT Laboratories (Haynos *et al.*, 1974), and resulted in a further boost in cell performance, taking terrestrial cell performance to above 17% (Fig. 4.3c). The surface features consisted of square-based pyramids defined by slowly etching {111} crystallographic planes. These greatly reduced reflection from the cell surface, giving these ‘black’ cells the appearance of black velvet after antireflection coating.

The improvements of the early 1970s came about primarily by improving the ability of the cell to collect carriers generated by the incoming photons. Since cells now appeared to be performing to close to their full potential in this area, it seemed that any further improvement in silicon cell performance would have to result from improved open-circuit voltage. Such improvement became the focus of work directed at increasing cell efficiency throughout the second part of the 1970s, largely as a result of a program directed by NASA-Lewis with this as a goal in order to improve space cell performance (Brandhorst and Bernatowicz, 1980).

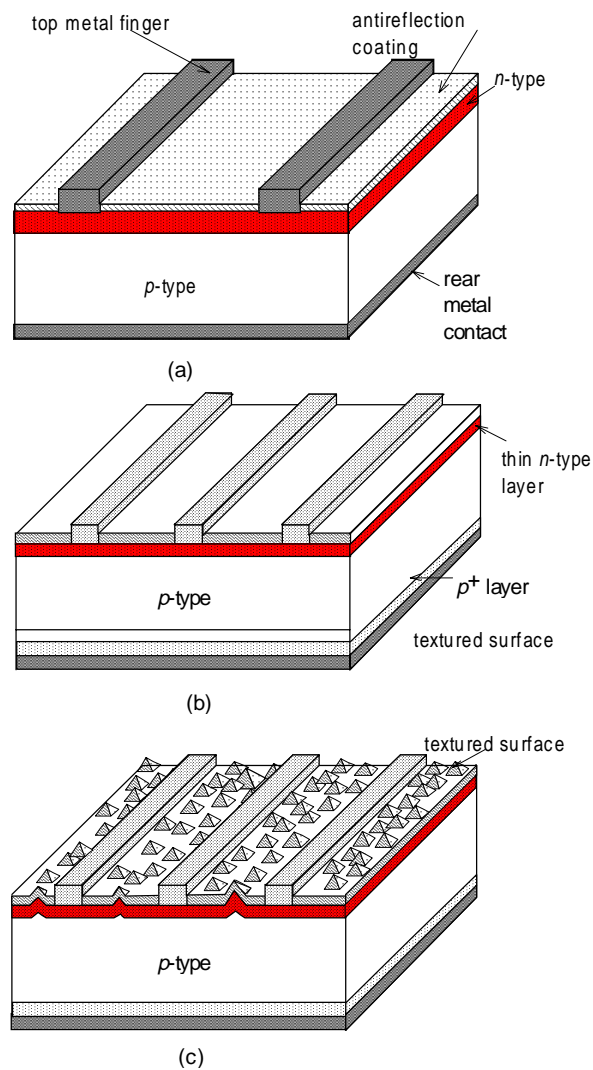


Figure 4.3 (a) Space silicon cell design developed in the early 1960s which became a standard design for over a decade; (b) shallow junction 'violet' cell; (c) chemically textured non-reflecting 'black' cell. Source: Green (1995).

On the commercial front, the oil embargoes of the early 1970s had generated widespread interest in alternative sources of terrestrial energy. A small terrestrial photovoltaic industry came into existence largely as a result of the US Government's photovoltaic program. One component of this program (Christensen, 1985), arguably the most successful in terms of developing the industry and its products, involved a staged series of purchases of photovoltaic modules meeting increasingly stringent specifications. The first such purchase in 1975/6, known as "Block I", was remarkable for the diversity of both cell fabrication approaches and module encapsulation approaches used in the product supplied by four different manufacturers. One manufacturer, Spectrolab of Sylmar, California, supplied cells where the contacts had been applied using screen-printing (Ralph, 1975), the forerunner of the millions of cells of this type which were to follow. In the "Block II" purchases under this program (1976/7), the same company combined screen-printed cells with a laminated module design (Fig. 4.1), a combined approach that had been adopted by almost all commercial manufacturers by the early 1980s and, with relatively minor modification, remains the present commercial standard.

The main features of a commercial screen-printed cell are shown in Fig. 4.4. The basic cell design is similar to that of a standard space cell of the 1960s (Fig. 4.3a), but incorporates the surface texturing of the 'black' cell of Fig. 4.3c as well, of course, as the screen-printing approach to applying the front and rear contacts.

Since the Block II purchases of 1976/7, no major changes have been made in either the basic screen-printed approach to cell fabrication or to the cell encapsulation approach until quite recently. Considerable attention, however, has been directed towards reducing the cost of the silicon wafer, usually grown by the Czochralski technique, since this accounts for about 40% of the cost of a standard silicon module. The most successful approach has been the simplification of the ingot growth processes by using cruder directional solidification or 'casting' approaches to produce multicrystalline ingots (Ferrazza, 1996). The first multicrystalline silicon cells developed specifically for the terrestrial market were reported in 1976 (Lindmayer, 1976; Fischer and Pschunder, 1976) and commercial multicrystalline cells have been available since the late 1970s. These multicrystalline approaches involve basically a reversion to the earlier ingot-forming approaches for crystal rectifiers, techniques pre-dating the microelectronics explosion. In 1998, multicrystalline silicon cells accounted for about 30% of the total market for photovoltaic product. Another major area of developmental emphasis has been to reduce the thickness of the silicon wafer by slicing it more thinly. This is resulting in a steady replacement of inner diameter sawing methods traditionally favoured by the microelectronics industry by wire cutting approaches, as described in more detail in Section 4.3.1.

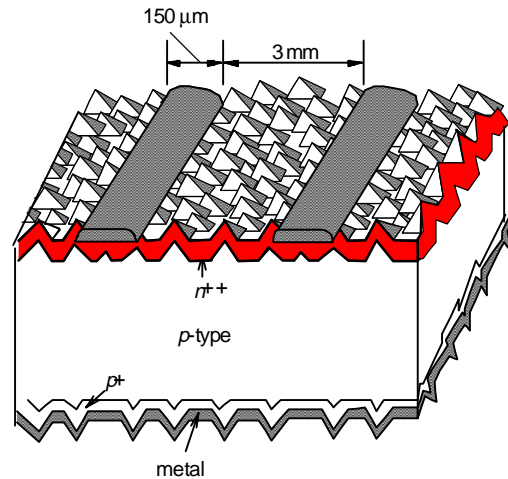


Figure 4.4 Screen-printed crystalline silicon solar cell (not to scale). Source: Green (1995).

On the research front, it had become apparent by the late 1970s that oxide passivation of the cell surfaces was the key to obtaining improved open-circuit voltage. The early 1980s saw a series of successively improved oxide-passivated cells fabricated by the author's group at the University of New South Wales (UNSW) taking silicon cell efficiency past 18%, then past 19% and finally 20%, the "four minute mile" of the photovoltaics area. The UNSW group has held the world record for silicon cell performance, almost without interruption, since this time.

The UNSW-developed microgrooved PESC cell (passivated emitter solar cell) of Fig. 4.5a was the first silicon cell to exceed 20% energy conversion efficiency in 1985. The same basic approach has since been used by several other groups to produce cells of similar efficiency, with commercial quantities produced for solar car racing and for space. The approach is characterised by the use of a thin thermally grown oxide to "passivate" (reduce the electronic activity of) the top surface of the junction diffusion (the emitter of the cell), combined with the use of a shallow, high sheet resistivity phosphorus diffusion for this emitter. Another is the use of photolithography to produce relatively small contact area to this emitter region by defining openings in the "passivated oxide". Photolithography is also used to pattern the top contact fingers and to align these fingers to the oxide openings. The rear of the cells borrows the "alloyed-aluminium back-surface-field" approach from earlier space cells. In this approach, a layer of aluminium is deposited on the rear of the cell and

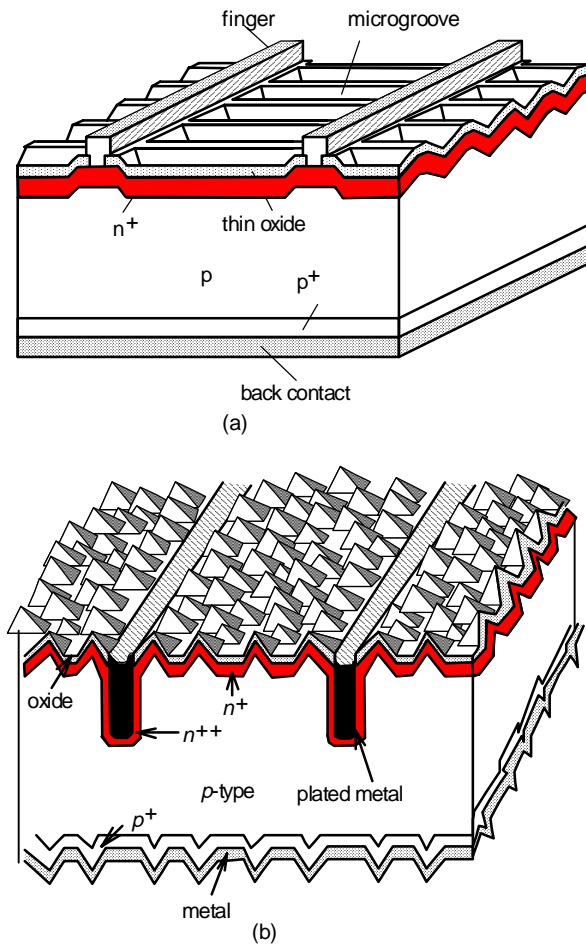


Figure 4.5 (a) The microgrooved passivated emitter solar cell (PESC cell) of 1985, the first silicon cell to exceed 20% efficiency; (b) buried-contact solar cell. Source: Green (1995).

alloyed into the cell at temperatures above the Si–Al eutectic. After cooling, this produces a layer of p -type Si heavily doped with Al at the rear of the silicon substrate. This reduces rear contact recombination rates. Some improvement of substrate quality also occurs during alloying by defect “gettering”. A parallel PESC approach had, prior to 1998, given the best results for multicrystalline silicon cells, with efficiencies up to 18.6% demonstrated on such material by this approach (Rohatgi *et al.*, 1996).

Cells of a similar quality to the first 20% efficient PESC cell have also found their way into high-volume terrestrial cell manufacture through the laser-grooved buried-contact cell of Fig. 4.5b. This cell retains an alloyed aluminium rear and also incorporates the improvements in front-surface passivation first demonstrated by the PESC cell. To make the approach suitable for low cost production, however, the photolithographic metallisation of the PESC cell is replaced by a unique combination of laser grooving, to define the areas to be metallised, followed by electroless metal plating. The oxide in this case not only serves as top-surface passivation, but it also serves as a diffusion mask to confine the heavy diffusion to the laser grooved areas and as a plating mask for the subsequent plating of metal into these grooved areas. In commercial versions of this sequence, the oxide can be replaced by a high-temperature dielectric such as silicon nitride, as discussed in more detail in Section 4.4. The buried-contact approach now produces the highest performance terrestrial cells that are produced in any appreciable volume, with efficiency in the 17–18% range routinely obtained using standard low-cost commercial silicon wafers.

The next major laboratory improvement in silicon cell design came in the use of oxide passivation along both the front and rear surfaces, as first demonstrated in the rear point contact solar cell developed by Stanford University. As shown in Fig. 4.6, this cell has an unusual design in that both positive and negative contact are made at the rear surface of the cell. Although this might, at first sight, appear to be a regression to a similar design to that used in the first modern silicon cell of Fig. 4.2c, there is a substantial difference in the way the two types of cells operate. For the modern rear contact cells, which take advantage of the excellent quality of silicon presently available, carrier diffusion lengths are several times the cell thickness, allowing carriers photogenerated near the top surface of the cell to diffuse to the rear contacts. In the earlier device, the junctions at top and rear surfaces are electrically connected by the junction around the cell edge. Most carriers in this earlier cell are collected by the top junction and flow around the edge of the cell to the rear contact, an approach that is only feasible for small area cells. The rear point contact cell demonstrated 22% efficiency in 1988 and has since been commercialised, finding use in photovoltaic systems which rely on concentrated sunlight and for high value-added applications such as solar car racing and high-altitude aircraft flights (Verlinden *et al.*, 1997).

The next improvement in silicon cell efficiency came, again at UNSW, by combining the earlier developments in the PESC cell sequence with the front and rear oxide passivation first demonstrated in the rear point contact cell. This is possible in a number of ways as shown in Fig. 4.7. In the PERC cell (passivated emitter and rear cell) of Fig. 4.7a, the first to be successfully demonstrated, rear contact is made to the

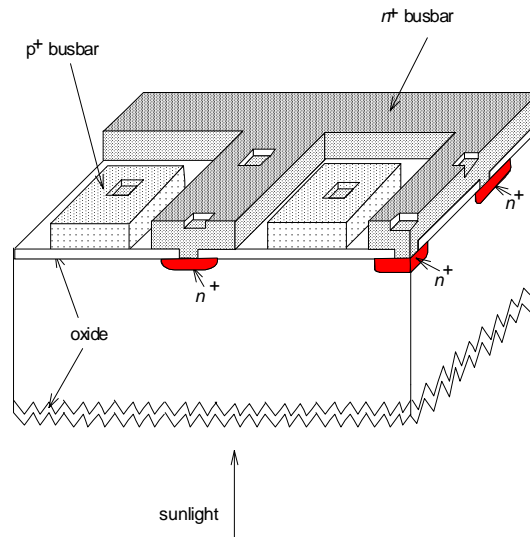


Figure 4.6 Rear point contact solar cell which demonstrated 22% efficiency in 1988 (cell rear shown uppermost). Source: Green (1995).

silicon substrate through holes in the rear passivating oxide. This approach works reasonably well provided the substrate is sufficiently heavily doped for contact resistance between the metal and substrate not to be an issue (below about $0.5 \Omega \text{ cm}$ resistivity for p -type substrates). The PERC cell is often suggested as a relatively low cost way for making silicon cells above 20% efficiency, since it is the simplest of the approaches of Fig. 4.7.

Historically, the next improvement was demonstrated by the PERL cell (passivated emitter, rear locally diffused cell) of Fig. 4.7b. In this case, local diffusion is used in the area of the rear point contact to provide a minority carrier-reflecting region between this contact and the substrate and to reduce contact resistance. This approach produced the first 24% efficient silicon cell in 1994 (Zhao *et al.*, 1995) and holds the current world record of 24.5% (Zhao *et al.*, 1998). The PERL cell has been used in reasonably large quantities in solar car racing and in space cells. The third cell of Fig. 4.7c is the PERT cell (passivated emitter, rear totally diffused). To date this has not given as good a performance as the PERL cell but it offers some fabrication simplifications. The PERT cell has also been used as the basis of space cell production.

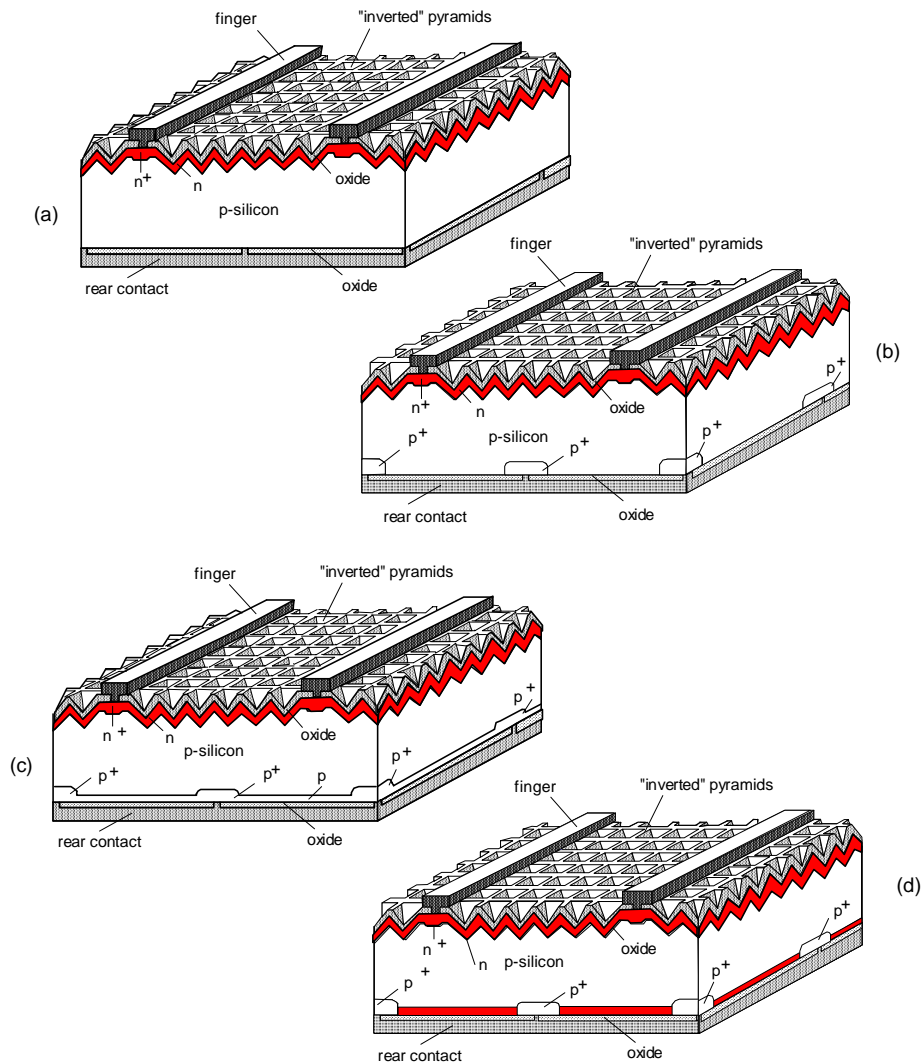


Figure 4.7 A family of four related high efficiency solar cell structures: (a) the passivated emitter and rear cell (PERC cell); (b) the passivated emitter, rear locally diffused cell (PERL cell) which took efficiency above 24% in the early 1990s; (c) the passivated emitter, rear totally diffused cell (PERT cell); and (d) the passivated emitter, rear floating junction cell (PERF cell). Source: Green and Hansen (1998).

The final structure shown in Fig. 4.7d, the PERF cell (passivated emitter rear floating junction) offers perhaps the best long-term potential for high performance. This structure has produced the highest open-circuit voltage silicon cells to date with open-circuit voltage up to 720 mV demonstrated under standard test conditions (Wenham *et al.*, 1994), together with efficiencies above 23%.

One feature of these more recent cell designs is the very effective trapping of light within the cell. By depositing metal over the entire rear surface of the cell but ensuring it is displaced from the silicon substrate by an intervening layer of oxide, very high rear reflectance for light striking this rear reflector structure from within the cell is obtained. When combined with appropriate geometrical structure on the front surface of the cell, weakly absorbed light that is reflected from this rear surface can be trapped quite effectively within the cell after total internal reflection from this front surface. This greatly extends the response of the cell to infrared wavelengths. Cells that convert such wavelengths with an efficiency approaching 50% have been demonstrated (Green *et al.*, 1992). Although oxide passivation remains the most effective technique for passivating cell surfaces yet demonstrated in experimental devices, recent work using wider band-gap amorphous or microcrystalline silicon layers has also produced encouraging results, as has work with specially deposited silicon nitride. A cell using an amorphous silicon emitter layer has been reported to give good performance (Tanaka *et al.*, 1993), although fundamentally limited to being less efficient than an oxide-passivated cell due to the poor electronic quality and the strong absorption in the amorphous silicon material. Similarly, cells with rear passivation using microcrystalline silicon layers instead of thermal oxide have produced quite encouraging results (Okamoto *et al.*, 1997) although they are also inherently not capable of matching the optical performance of oxide passivated devices due to parasitic absorption in the microcrystalline layer. Excellent surface passivation properties have also been reported for silicon nitride deposited by a remote plasma approach (Aberle *et al.*, 1997).

How will cell design evolve in the future? Some insight is provided by Fig. 4.8, which shows the calculated intrinsic energy conversion efficiency bounds on single-junction silicon solar cells, with and without 'lambertian' light trapping. In 'lambertian' light trapping schemes, the light direction within the cell is randomised (Green, 1995) allowing path-length enhancements to be quite readily calculated (about 50 in idealised situations). The best laboratory cells have demonstrated close to 85% of the achievable efficiency, according to this figure. In the best experimental devices, performance losses of the order of 5% arise from less than ideal values of each of the short-circuit current, open-circuit voltage and fill factor parameters. The short-circuit current losses are most easily identified and reduced. These come from metal finger

coverage of the top surface, top-surface reflection loss, and less than perfect light trapping in the experimental cells. The voltage loss arises from finite surface and bulk recombination in excess of the lower limit imposed by intrinsic Auger recombination processes (Green, 1984). The fill factor loss comes not only from ohmic series resistance loss within the cell, but also from the same factors producing the open-circuit voltage loss. To eliminate the latter, parasitic recombination must be sufficiently reduced so that the dominant recombination component at the cell's maximum power point is Auger recombination. This is a more challenging requirement than the corresponding criterion at open-circuit voltage (Green, 1984).

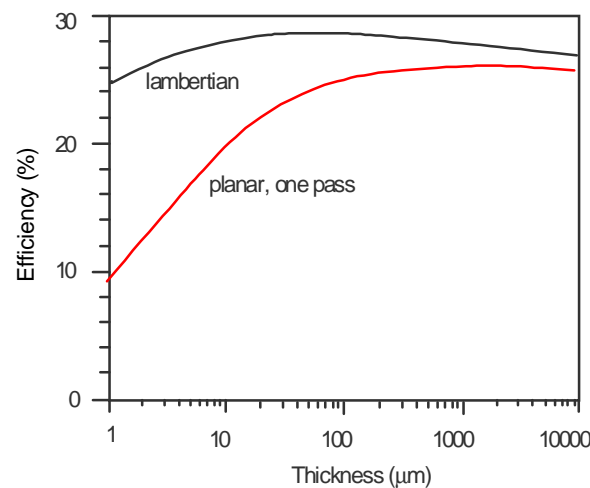


Figure 4.8 Limiting efficiency of a silicon solar cell as a function of cell thickness with and without lambertian light trapping (global AM1.5 spectrum, 100 mW cm^{-2} , 25 C). Source: Green (1995).

As opposed to the case of laboratory devices, most manufacturers of commercial cells would be very pleased to be producing consistently cells of half the limiting efficiency of Fig. 4.8. Some of the difference between laboratory and commercial cell performance is due to poorer quality of silicon substrate material. A large component, however, is due to limits imposed by the present screen-printing process predominantly used for commercial cell fabrication. The penalty for the processing simplicity offered by this approach is a compromised cell design, since a heavily doped emitter layer appears unavoidable. Improved designs such as the buried-contact cell offer the seemingly contradictory advantages of both higher cell performance and lower overall manufacturing costs.

It seems that eventually it should be feasible to produce low-cost commercial silicon cells of efficiency above 20% with such improved cell designs by paying attention to the passivation of both front and rear surfaces, by thinning the cells to reduce bulk recombination and by modifying the crystal growth processes to produce low-cost silicon customised for photovoltaics, particularly in its ability to withstand high-temperature processing without loss of electronic quality.

An interesting result highlighted by Fig. 4.8 is the way that light trapping allows high performance, in principle, from silicon cells that are only $1\text{ }\mu\text{m}$ thick. This provides a justification for expecting very high performance, eventually, from the thin, supported silicon cells discussed in Section 4.7. To approach the limiting performance, the demands on bulk quality become less severe as the cell becomes thinner (Green, 1995). However, those upon light trapping and surface passivation become more severe.

Various approaches have been suggested which have the potential, in principle, for exceeding even the efficiency limits of Fig. 4.8. These include the use of tandem cells, the use of high-energy photons to create more than one electron-hole pair (Werner *et al.*, 1994), or the use of sub-band-gap photons in schemes such as incorporation of regions of lower band gap (Healy and Green, 1992), multiple quantum wells (Barnham and Duggan, 1990) or mid-gap impurity levels (Wolf, 1960). Experimentally, the tandem cell approach appears the most likely to have impact in the long term, once the problems with lattice-matching a top cell to silicon with a suitable band gap are overcome. Promising results have been demonstrated with a-Si/c-Si tandem cells, although a better performing top cell will be required in the longer term to retain a performance advantage over that offered by the rear cell alone.

4.3 Substrate production

4.3.1 Standard process

Not only is silicon solar cell technology capable of benefiting directly from the economies of scale of the silicon microelectronics industry, but also it is capable of using scrap material from this industry because the requirements for material quality in photovoltaics are less demanding than in the more general microelectronics field. Until the photovoltaic industry requires a larger volume of silicon than the microelectronics industry, it will be difficult for approaches customised for photovoltaics to compete with the costs of reject silicon from microelectronics. Accordingly, given the present size relativities, most silicon cells are made from

standard silicon source material originally intended for microelectronics. Over the last ten years, the size relativities have not changed enormously, since both industries have been steadily growing. Explosive growth in the photovoltaics industry, such as that stimulated by urban residential rooftop applications of photovoltaics in 1997, will increasingly upset this delicate balance.

For microelectronics, the starting point for producing the requisite high quality “semiconductor grade” silicon is a lower grade of silicon known as “metallurgical grade”, produced by the reduction in an arc furnace of quartzite by carbon, the latter generally in the form of wood chips. This metallurgical grade silicon is of about 98% purity and is produced in large quantities for the steel and aluminium industries. A relatively small quantity is refined for microelectronics by conversion to a volatile intermediary that can be purified by fractional distillation. The purified intermediate compound is then decomposed to re-extract the silicon in a highly purified form. Generally the metallurgical grade silicon is converted by hydrochloric acid to trichlorosilane, which is then purified to 99.9999999% (nine “nines”) purity by fractional distillation. Silicon is then extracted from the trichlorosilane by reducing the latter by hydrogen at high temperature. In this process electrically heated silicon rods are exposed to a trichlorosilane/hydrogen mixture which reacts on the surface of the rods, depositing silicon onto them and hence building up their cross section. These rods grow with a fine-grain polycrystalline silicon microstructure. After the rod diameter has increased to the required size, the process is stopped and the rods mechanically broken into smaller chunks, which maintain “nine-nines” purity. These chunks then become the starting point for the growth of ingots of good crystalline quality. As previously mentioned, crystalline ingots are generally grown by the Czochralski process. In this process, the purified silicon chunks are melted in a quartz crucible along with small pieces of silicon heavily doped with boron. This produces a boron-doped melt into which a seed crystal is dipped and slowly withdrawn (Fig. 4.9a). For high quality crystal growth, good temperature uniformity and slow and steady growth are required. Typically ingots are grown to about 10–15 cm in diameter and 1–2 metres in length, weighing 50–100 kg. The crystallographic orientation of the seed is transferred to the grown crystal. Generally, for photovoltaics, the crystal is grown with a preferred orientation so that the wafers which are sliced from the crystal perpendicular to the growth axis have surfaces parallel to {100} crystallographic planes.

Prior to slicing these ingots into wafers, the ingots are generally subject to a centreless grinding operation to remove the slight fluctuations in diameter along the length of the ingot that occur during crystal growth.

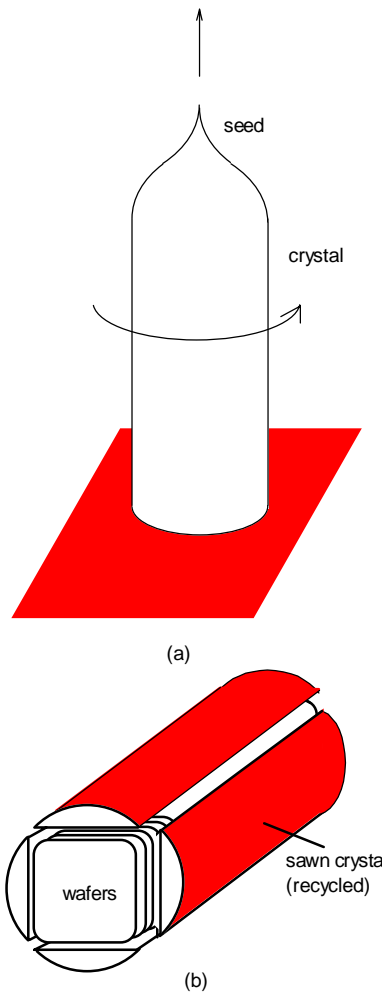


Figure 4.9 (a) Czochralski (CZ) growth; (b) squared-off CZ ingot. Source: Green and Hansen (1998).

Alternatively, the ingots can be “squared-off” by sawing off large sections parallel to the growth axis (Fig. 4.9b), giving “quasi-square” wafers after wafering. The large pieces of silicon sawn off in this approach are then generally recycled by re-melting as feedstock for the CZ growth.

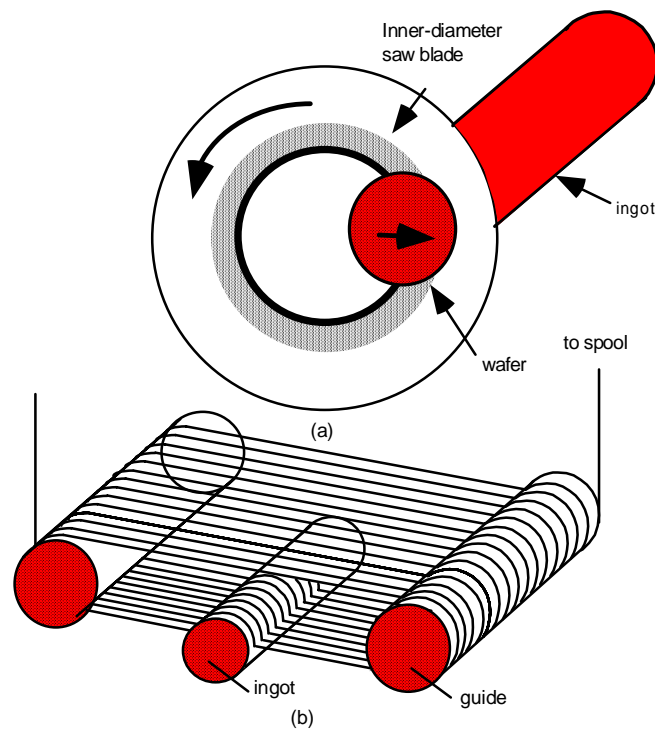


Figure 4.10 (a) Inner diameter wafer sawing; (b) continuous wire sawing. After Dietl *et al.* (1981).

The technique traditionally used in microelectronics for sawing wafers from ingots has been based on the use of inner diameter saws. In this technique, shown Fig. 4.10a, thin metal sheet blades are given dimensional solidity by being held in tension around their outer perimeter. The cutting surface is a diamond-impregnated region surrounding a hole within the tensioned metal sheet. This technique gives excellent dimensional tolerance, although there are limitations arising from the thickness of the silicon wafers that is possible to produce while still maintaining high yield. Other limitations arise from the wastage of silicon as “kerf” loss during cutting. Generally, about 10–15 wafers per centimetre of ingot length are achieved by this process. An alternative technique increasingly being used in photovoltaics is based on wire sawing (Fig. 4.10b). In this case, tensioned wire is used to guide an abrasive slurry through the ingot. Advantages are thinner wafers and less surface damage for these wafers as well as lower kerf or cutting loss, allowing the sawing of over 20 wafers per centimetre.

In the 1970s and early 1980s, several other options for preparing silicon feedstock were investigated as part of a large US government PV program encouraged by the Carter administration (Christensen, 1985). A great diversity of alternative routes to producing pure silicon were investigated. These ranged from those involving radically different approaches to those exploring only minor changes from the sequence outlined above, such as the use of different compounds of silicon as the intermediate during the purification process. One such process, based on the use of silane as the intermediate (Christensen, 1985), is now being used commercially, although the product is used exclusively for the microelectronics industry. Parallel development has been conducted outside this program, notably in Germany (Aulich, 1996) and Japan. In Japan, Kawasaki Steel have been investigating an alternative route to preparing cheap silicon feedstock from metallurgical grade precursors and were scheduled to begin pilot production with this sequence in 1998 (Sakaguchi *et al.*, 1997).

To produce ingots from the pure silicon feedstock, a modification of the CZ process which produces “tricrystalline” silicon has also been used for photovoltaics (Endrös *et al.*, 1997). Wafers cut from the crystals have a different {111} equivalent orientation for each third of their surface, with the differently orientated regions separated by a twinning plane. Claimed advantages of higher growth rates and greater mechanical strength are probably not large enough to offset disadvantages of not being able to chemically texture such wafers and the poor electronic quality near the twinning planes. Another alternative to the standard Czochralski process for producing crystalline ingots is the floatzone (FZ) process. Although some studies have predicted superior economics when compared with the Czochralski process for cell production due to the elimination of consumables such as quartz crucibles, the FZ process, as commercially implemented, is capable of accepting feedstocks only in the form of high quality cylindrical rods. This makes it unsuitable for using low-cost off-grade material. However, the casting and directional solidification processes used to produce multicrystalline silicon are generally extremely tolerant of poor quality feedstock material. These techniques will be discussed in more detail in the following section.

4.3.2 Multicrystalline silicon ingots

In 1998, about 30% of the world’s photovoltaic production was based on multicrystalline silicon wafers. Several companies have developed commercial processes for producing the precursor multicrystalline silicon ingots (Ferrazza, 1996). Advantages over the Czochralski process are lower capital costs, higher throughput and a higher tolerance to poor feedstock quality.

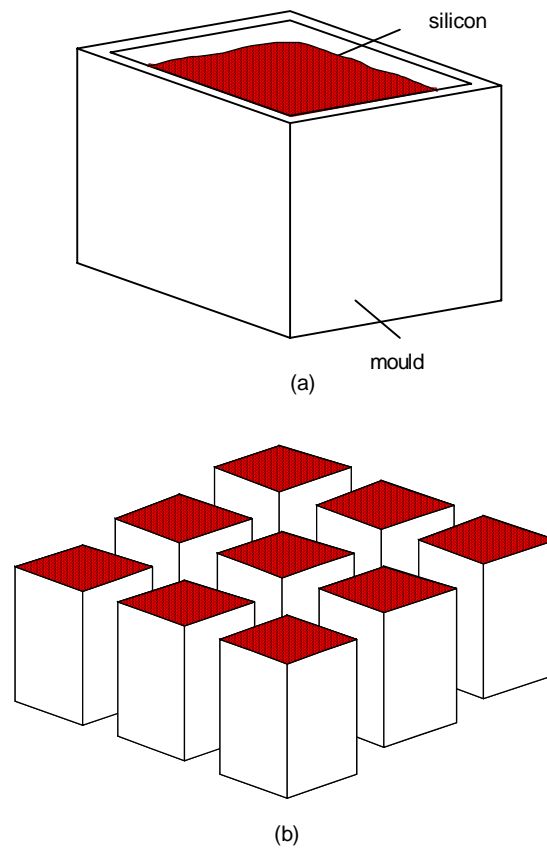


Figure 4.11 (a) Directional solidification of silicon within a mould; (b) sawing of large ingot into smaller sub-sections. Source: Green and Hansen (1998).

The technique involves controllably solidifying molten silicon in a suitable container to give silicon ingots with large columnar grains generally growing from the bottom of the crucible upwards (Fig. 4.11a). Pioneers with this approach for modern photovoltaics in the mid-1970s were Wacker Chemitronic of Germany (Authier, 1978) and Solarex of the USA (Lindmayer, 1976). In the 1980s, other manufacturers including Eurosolare/Crystallox, Kyocera, Bayer, Crystal Systems and Sumitomo Sitex had developed processes capable of producing good quality multicrystalline material. Techniques differ between these manufacturers in the choice of crucible material, the method of loading the crucible with silicon and the method for controlling the cooling of the melt. A good summary can be found elsewhere

(Ferrazza, 1996). The size of a nominally rectilinear ingot can be very large, up to 60 cm × 60 cm × 20 cm, and these ingots can weigh several hundred kilograms (Khattak and Schmid, 1997). The large ingots are sawn into smaller sections as shown in Fig. 4.11b, eventually to give wafers generally 10–15 cm along the sides. These smaller sections can be sawn by the standard inner-diameter or continuous wire sawing processes. The resulting multicrystalline wafers are capable of producing cells of about 80% of the performance of a monocrystalline cell fabricated on a CZ wafer. However, because of the higher packing density possible due to their square or rectangular geometry, this performance difference is largely masked at the module level with multicrystalline module performance lying in the range demonstrated by modules made from monocrystalline cells.

An interesting variation on this approach is the continuous casting process such as developed by Sumitomo Sitex. In this case, electromagnetic fields are used to constrain the molten silicon to produce essentially a continuous ingot of multicrystalline silicon (Sarti *et al.*, 1997).

4.3.3 Sheet and ribbon silicon

Although there is the potential for substantial cost reductions in both the cost of preparing the silicon feedstock and in forming crystalline or multicrystalline ingots from it, one unavoidable cost with the silicon wafer approach is the cost of sawing the ingot into wafers. Several studies have suggested that the lower bound on this cost may be something of the order of US\$0.20/watt (Christensen, 1985; Bruton *et al.*, 1997). This has provided the rationale for investigating approaches that produce silicon directly in the form of self-supporting sheets without the need for sawing (Bergin, 1980; Shulz and Sirtl, 1984).

Commercially, the most advanced sheet or ribbon approach is based on the edge-defined film-fed growth (EFG) technique of Fig. 4.12. As originally developed in the early 1970s, this involved the pulling of a thin sheet of silicon ribbon from a strip of molten silicon formed by capillary action at the top of a graphite dye (Fig. 4.12a). Substantially higher throughput was obtained with the more symmetrical configuration shown in Fig. 4.12b, where the ribbon is pulled in the form of a hollow nonagon. Individual wafers are then cut from the sides of the nonagon, normally by laser scribing wafers from each of the sides. The material produced is multicrystalline with elongated grains and of a similar quality to the standard directionally solidified multicrystalline material. Commercial cells made from EFG material have been available sporadically since the early 1980s with a large 25 MW/yr facility recently announced.

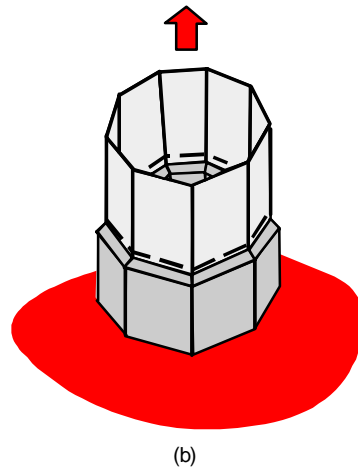
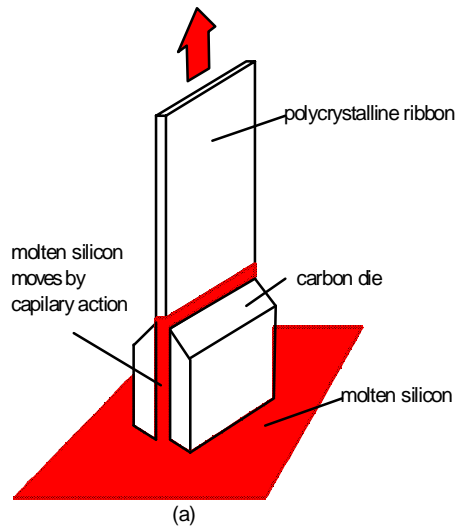


Figure 4.12 (a) Edge-defined, film-fed growth (EFG) method; (b) growth of a nonagonal ribbon of silicon using the EFG method. Source: Green and Hansen (1998).

An even older ribbon growth process is the dendritic web approach of Fig. 4.13 first described by Westinghouse in the 1960s. In this approach, close thermal control is used to cause two dendrites spaced several centimetres from each other to solidify first during the growth step. When these are drawn from the melt, a thin sheet of molten silicon is trapped between them. This quickly solidifies to form a ribbon. After a substantial research and demonstration program by Westinghouse in the 1970s and early 1980s, this approach is now under development by Ebara Solar (Narashima *et al.*, 1997).

A somewhat related approach is the string ribbon approach. In this case, the molten silicon is trapped between two graphite strings that are drawn from the melt. This relaxes the requirement on thermal control, compared with the previous dendritic web approach. The string ribbon approach is under development by Evergreen Solar (Janoch *et al.*, 1997; Wallace *et al.*, 1997).

Another interesting approach that was developed in the 1980s relied on direct casting of silicon wafers using a centrifugal casting approach to overcome surface tension problems within the closely spaced faces of a horizontally aligned graphite mould (Maeda and Hide, 1987). Despite initially promising results, this approach appears to be no longer under active development. A compact but thorough review of most of the above ribbon processes including references is given elsewhere (Shulz and Sirtl, 1984). A thorough bibliography of work prior to 1980 has also been published (Bergin, 1980).

Somewhat related to the above ribbon approaches are other sheet approaches which produce silicon films on substrates from which they are subsequently detached. The most developed version of this technology is the VEST technology developed by Mitsubishi (Hamamoto *et al.*, 1997). In this approach, a potentially reusable silicon substrate is oxidised, then vias are etched in the oxide and then a silicon film is deposited on top of the oxide. This film is subsequently laser-recrystallised. The thickness of this seeding layer is then increased by the subsequent high-temperature epitaxial growth of the silicon layer. After reaching a target thickness of 50–80 μm , the film is detached from the substrate which is then potentially reusable. Promising efficiencies over 16% have been obtained from this approach for substrates that are only 60–70 μm in thickness, but are still self-supporting. Other researchers have suggested similar techniques to produce even thinner films. Some have suggested the use of a silicon wafer treated to produce a layer of porous silicon along the surface as the source of the crystallographic template for the subsequent growth of a silicon layer, which is then detached (Wenham and Green, 1995; Brendel, 1997). If this detached layer is too thin to be self-supporting, it could be transferred to structurally strong components such as the glass layer in a structural superstrate design. Another

variant involves forming vias through the oxide to a {100} orientated substrate and the subsequent use of liquid phase epitaxy to grow a mesh of silicon on the substrate which again is detached after processing (Weber *et al.*, 1997). In this case, layers of about 70 μm thickness are envisaged, although cell processing on the unusual geometries that result would pose obvious challenges.

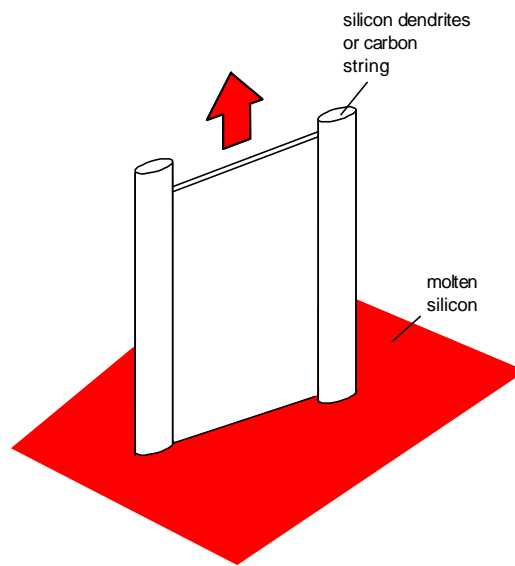


Figure 4.13 Schematic illustrating either the dendritic web growth process or the string ribbon approach. Source: Green and Hansen (1998).

4.4 Cell processing

4.4.1 Standard process

In the previous section, standard and non-standard ways of forming the silicon substrate were described. The major commercial substrates are those formed by the wafering of monocrystalline and multicrystalline ingots, with a much smaller quantity of EFG ribbon substrates produced commercially. Since monocrystalline silicon wafers are the norm, processing for these will be described first with the processing of other types treated as variations on the monocrystalline processing approach.

At present, no photovoltaic manufacturer prepares polysilicon source material. Manufacturers generally purchase off-specification material from the microelectronics industry or, alternatively, bypass the crystal growth step by purchasing silicon wafers. Processing starts by chemically cleaning the starting wafers and etching their surfaces, generally in a sodium hydroxide etchant, to remove saw damage from the wafers. For monocrystalline wafers, the next step is crystallographic texturing, again using sodium hydroxide but in a more dilute solution. The composition and temperature of this solution determines the texturing quality (King and Buck, 1991), including the size of the pyramidal features resulting from the texturing and the percentage of wafer surface area successfully covered by such features. Texturing is a demanding step in cell processing and the quality of texturing varies enormously between different manufacturers. Cell performance, however, is not critically dependent on texturing quality.

The next major stage of processing is the diffusion of the cell junction. This is generally achieved by spraying or spinning a compound containing phosphorus onto the cell surface, followed by heating at high temperature to allow phosphorus dopant atoms to seep into the cell surface by thermal diffusion. Typically, the depth of diffusion is less than 1 μm . The same thermal diffusion process is widely used in microelectronics but processing for photovoltaics generally involves cruder equipment and techniques, since the aim is to produce cells at the lowest possible cost without unduly sacrificing cell performance. Although the diffusion is required over only one surface of the wafer and processing techniques are generally chosen to encourage such a result, phosphorus invariably seeps into both wafer surfaces to some extent.

To break the connection between the phosphorus diffused into front and rear surfaces, an 'edge junction isolation' step is required to remove the thin phosphorus layer around the edge of the wafer. This isolation is often achieved by 'coin stacking' the wafers so that only their edges are exposed and then placing the stack in a plasma etcher to remove a small section of silicon from the wafer edge, hence breaking the conductive link between front and rear surfaces.

The screen printing of metal contacts onto the front and rear surfaces completes cell processing. Silver paste consisting of a suspension of fine particles of silver and glass frit in an organic medium together with appropriate binders (Hoernstra *et al.*, 1997) is squeezed through a patterned screening mesh onto the cell surface. After application, the paste is dried at low temperature and then fired at a higher temperature to drive off the remaining organics and to allow the silver regions to coalesce. The glass frit is important in promoting adhesion to the silicon substrate. Often pastes are doped with phosphorus to help prevent the screened contact from penetrating the thin phosphorus skin that it is intended to contact.

The paste for the top surface is printed in a characteristic finger pattern to minimise the resistive losses in the cell while allowing as much light as possible into it. Sometimes the rear contact is patterned, not to allow light into the cell, but merely to reduce the amount of paste required and hence reduce the cost of this processing step. Sometimes small quantities of aluminium are added to the paste used on the rear surface to give a heavily doped *p*-type 'back-surface field' region underlying the rear metal contact or, alternatively, separate screening and firing of an Al paste over the entire rear surface is used to more fully optimise this feature (Nijs *et al.*, 1996).

This screen-printing method for applying the metal contact was borrowed in the early 1970s from the hybrid microelectronics industry (Ralph, 1975). This ensured the ready availability of both screen-printing equipment and the paste-firing furnaces suited to this application. Labour and equipment costs associated with this step tend to be very low. However, the pastes themselves can be expensive and an even larger cost penalty is paid for the simplicity of this approach by the forfeiture of the inherently available power output from the silicon wafer, as discussed later.

A quarter wave antireflection coating can be applied to the cell at this stage. Generally, titanium dioxide is used as the antireflection coating material due to the simplicity of depositing this compound and its almost ideal refractive index for this application. Some manufacturers deposit the antireflection coating before the metal paste-firing step and fire the paste through this coating.

The cells are then ready for testing under a solar simulator. Cells are usually graded based on their short-circuit current or current at a nominal operating voltage, *e.g.*, 450 mV. Generally, cells are sorted into 5% performance bins. This sorting is required to reduce the amount of mismatch within the completed module. To a large extent, the output current of the module is determined by that of the worst cell in the module, resulting in large power losses within mismatched modules. Even worse, low output cells can become reverse-biased under some modes of module operation and destroy the module by localised over-heating.

Very similar processing is applied to multicrystalline silicon wafers. In this case, most of the grains will have incorrect orientation for effective texturing by anisotropic etching, although such texturing is sometimes used for the relatively small benefit that can be obtained. However, a quarter-wave interference antireflection coating has been mandatory for good performance from multicrystalline materials. One disadvantage of anisotropic texturing of these materials is that different grains etch at different rates, giving a very uneven surface due to steps at grain boundaries. This can pose hazards for continuity of the subsequently screened metal lines. Accordingly, some manufacturers prefer to etch multicrystalline silicon with an isotropic etch to maintain a smooth surface.

The rippled surface that is a natural consequence of the EFG ribbon growth process poses similar continuity hazards for screen-printed metallisation. To accommodate this rough surface, a novel technique has been developed whereby the metal paste is squeezed through an orifice and then drops to the cell surface, much the same as squeezing toothpaste from its tube onto a toothbrush.

4.4.2 *Limitations of the screen-printing approach*

There are four main limitations arising from the screen-printing approach to applying the front contact that cause the simplicity in processing to be at the expense of cell performance. As noted above, performance can be reduced well below that inherently achievable. One limitation is that the phosphorus diffusion has to be heavier than desirable purely from the point of view of cell performance, to allow reliable low resistance contact between the screen-printed metal and the diffusion. Typically, sheet resistivities of this diffusion less than 60 ohms/square are required (Green, 1995; De Clercq *et al.*, 1997). Such diffusions generally reduce the quality of the silicon in the region near the cell surface where blue wavelengths in sunlight are strongly absorbed. A screen-printed cell does not therefore respond well to blue wavelengths in sunlight, wasting at least 10% of the possible current output through this deficiency. The remaining three limitations relate to the geometry and conductivity of the metal lines it is possible to produce by the standard screen-printing process. Since the paste thickness shrinks to about one-third of its original thickness during firing (silver constitutes only 25–30% by volume of the original paste, with up to 5% glass frit), it is very difficult to achieve metal lines with high aspect ratio (height/width). High aspect ratios are the key to designing metal grids that result in low overall losses (Serreze, 1978). The nature of the screening meshes that have sufficient ruggedness for use in commercial production means it is very difficult to achieve fine lines using screen printing in production. Typically, 150 μm is the minimum width that can be cost-effectively achieved. This limitation means that there will generally be high shading losses in screen-printed cells due to the large percentage (10–15%) coverage of the front surface by the metal. Additionally, the relatively poor conductivity of the fired silver paste—about 2 times lower than that of pure silver for large features such as busbars but up to 6 times lower for finer features such as fingers (de Moor *et al.*, 1997)—fundamentally limits ability to optimise metal contact design, in much the same way as does the low aspect ratio previously discussed.

Recent work describes improved laboratory cell performance based on experimental screens formed by cutting patterns in thin metal sheets using a laser (Nijs *et al.*,

1996). This approach is reported to allow reduced linewidths, although the authors may be overly optimistic about the potential in a production setting (de Moor *et al.*, 1997). With a standard sequence under laboratory conditions, cell efficiency is limited to less than 15% even with these improved linewidths (Nijs *et al.*, 1996). In a more complex sequence involving inherently costly steps such as the deposition of a plasma nitride antireflection coating and a complicated rear Al screening and removal step, efficiency approaching 17% has been confirmed. Some caution is required in accepting the authors' enthusiasm as to how transferable these sequences may be to a production setting. The same authors (Nijs *et al.*, 1996) also analyse cost and performance relative to established commercial sequences such as the buried-contact sequence described below but these analyses appear to be skewed by overly optimistic assumptions about screen-printing metallisation parameters.

4.4.3 Buried-contact solar cells

As mentioned in Section 4.2, buried-contact cells were developed as a way of incorporating some of the efficiency improvements demonstrated in the mid-1980s into low-cost commercial cell production sequences. This aim has been successfully realised with recent independent costing studies showing that the buried-contact cell not only produces the highest commercial silicon cell efficiency, but also the lowest cost approach for fabricating commercial silicon cells, of any of those at any reasonable state of development (Bruton *et al.*, 1997).

The processing of buried-contact cells begins similarly to that outlined for screen-printed cells. In the commercially most successful buried-contact sequence (Jordan and Nagle, 1994), the incoming wafers are cleaned and textured as with conventional wafers and then diffused. A silicon nitride antireflection layer is grown by chemical vapour deposition over the entire top surface of the cell. Grooves are next formed in this surface through the antireflection coating and prior diffusion. A standard neodymium YAG laser readily produces grooves of about 20 μm width. The depth depends on the laser power, but desirably lies in the range 20–60 μm . After etching to clean the grooves, a second diffusion, which is restricted by the nitride to the regions that have been laser-grooved, is performed. Aluminium is then evaporated onto the rear of the wafer and sintered. Electrolessly plated nickel followed by similarly applied copper and silver is then deposited. Again, the insulating nitride restricts the plating to the grooved areas and to the rear of the wafer which has already been metallised by aluminium.

When applied to the same commercial silicon wafers as used in the screen-printing process, cell efficiencies in the 17–18% range are obtained. Figure 4.14 compares the performance of a screen-printed and a buried-contact cell fabricated on the same quality starting material (BP Solar, 1991). A performance advantage of 20–30% is demonstrated by the buried-contact approach, largely as a result of improved short-circuit current density but with other significant contributions coming from improved fill factor and open-circuit voltage. In addition to this performance advantage under standard test conditions, field studies have shown that buried-contact cells give up to 15% more energy per rated watt as a result of an even larger performance margin at low light intensities and under the bluer light associated with cloudy conditions (Mason *et al.*, 1997).

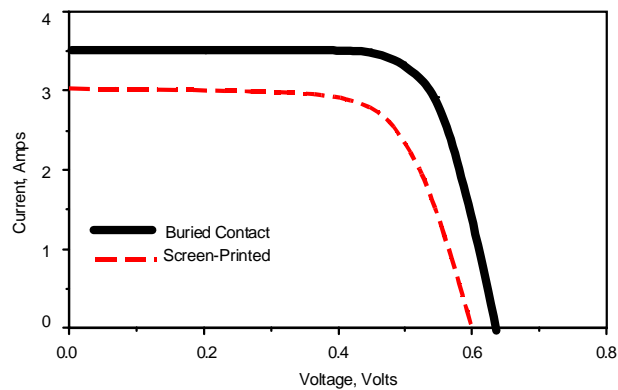


Figure 4.14 Output characteristics of buried-contact cells compared with screen-printed cells. After BP Solar (1991).

4.5 Cell costs

There have been many studies of the costs of the different stages of silicon cell production using different basic assumptions, particularly in relation to the production volume assumed in the study and the cost of polysilicon source material. Probably the most recent and most authoritative is one conducted under the auspices of the European Union Photovoltaic Program (Bruton *et al.*, 1997). This study involved representatives of seven major European photovoltaic manufacturers and research laboratories, and is valuable for the breadth of representation and the diversity of approaches explored. Since the groups involved are known for their strong views on the virtues of the different sequences studied, the study also involves an undoubtedly

hard-won political and technical consensus of those intimately involved with these issues.

The key assumptions of the study were manufacturing volume of 500 MW_p of solar cells per annum and the availability of silicon source material at US\$25 per kg. A number of different technologies were compared. Important comparisons were between EFG ribbon, multicrystalline and crystalline wafer technologies, between screen-printed, buried-contact, metal–insulator–semiconductor and PERL cell processing sequences, in various combinations of wafers and processing, and between two different module encapsulation approaches. However, the results from all possible combinations were not studied (or, at least, not published), but only the seven selected combinations shown in Table 4.1.

Table 4.1 Summary of published results of a European Commission study of manufacturing costs for 500 MW_p per year factory

ID	Wafer ^a	Process	Cell efficiency ^b study (present)	Estimated cost (ECU/W _p) ^c	Key variable
#1	DS	SP	15% (12.6–14.8%)	0.91	Wafer
#2	CZ	SP	16% (13.9–15.6%)	1.25	Wafer/process
#3	CZ	LGBC	18% (16.5–17.5%)	1.15	Process
#4	CZ	MIS/A	17% (N/A)	1.28	Process/module
#5	CZ	MIS/B	17% (12.2%)	1.34	Module
#6	CZ	PERL	20% (N/A)	1.78	Process
#7	EFG	SP	14.4% (12%)	0.71	Wafer

^aDS: directional solidification; CZ: Czochralski growth; EFG: edge-defined film-fed growth; SP: screen-printed; LGBC: laser grooved, buried-contact; MIS/A: metal–insulator–semiconductor; MIS/B: as for MIS/A but with resin-fill packaging; PERL: passivated emitter, rear locally diffused (less appropriate acronym LBSF used in study). ^bThe cell efficiencies assumed in the study in some cases differ appreciably from present average production values, deduced by the present author from manufacturers' data sheets or the results from large field installations. ^c1ECU ≈ US\$1.2.

Source: Bruton *et al.*, 1997.

Several key results can be deduced from this Table. When comparing screen-printed cells on ribbon (EFG), multicrystalline (DS) and monocrystalline (CZ) wafers, the ribbon produces the lowest cost of 0.71 ECU/W_p followed by the multicrystalline wafers at ECU0.91/W_p and the monocrystalline wafers at ECU1.25/W_p. The advantage of the ribbon stems almost entirely from the fact that it does not need to be sawn, as previously mentioned.

Comparing between the different processing approaches on single crystal wafers, the cheapest is the buried-contact at 1.15 ECU/W_p, followed by the screen-printed at 1.25 ECU/W_p, followed by the metal–insulator–semiconductor at 1.28 ECU/W_p, followed by the PERL at 1.78 ECU/W_p. The buried-contact achieves its cost advantage over the screen-printing approach by virtue of the increased efficiency giving more power per unit processing area. Such advantages would transfer to the less expensive substrate approaches studied, suggesting the best possible combination of wafer, process and moduling approach would result in manufacturing costs well below 0.70 ECU/W_p. In the module area, the standard laminated module approach is calculated to be slightly cheaper than an alternative resin-fill approach. Compared to the predictions of this study, present manufacturers fabricate screen-printed monocrystalline and multicrystalline cells and buried-contact monocrystalline cells in roughly 10–20 MW_p per year production capacities with large-volume selling prices of modules in 1999 of about US\$4/W_p (a similar amount in ECU/W_p). Present encapsulated cell efficiencies, deduced by the present author mainly from manufacturers' data sheets or from recent field performance, are also shown in Table 4.1, indicating the various levels of extrapolation in cell performance assumed for the different cell technologies in the study.

4.6 Opportunities for improvement

4.6.1 Commercial cells

The large differential between the efficiencies of a typical screen-printed commercial cell (15%) and the best laboratory silicon cell (24%) shows the enormous potential for further efficiency improvement in commercial devices. Part of this potential has been recently realised with the commercialisation of the buried-contact cell with cell efficiencies in the 17–18% range obtained in production. There remains scope for a further substantial performance improvement.

One reason for the difference between laboratory and the best commercial cells is the difference between the CZ wafers used in commercial production and the FZ wafers used for the best laboratory cells. CZ grown wafers are invariably contaminated with oxygen and carbon during growth to a much higher level than FZ wafers, due to use of quartz crucibles and graphite heaters in the CZ process. These impurities give rise to a much more subtle dependence on processing conditions, in the CZ material, of an important silicon material property for producing high performance cells, the minority carrier diffusion length. For example, applying the

high temperature processing associated with PERL type sequences to CZ silicon gives a large spread in results depending on the supplier of CZ material and hence most probably on the oxygen and carbon content (Wettling *et al.*, 1996). Additionally, the quality of CZ material as compared with FZ falls off quite rapidly as the boron content is increased, possibly because boron/oxygen complexes form within the material. This reduces flexibility in cell design since it eliminates the possibility of using low resistivity CZ substrates.

In microelectronics, high oxygen content resulting from the CZ process is regarded as an asset. Oxygen increases the mechanical strength of the wafers as well as allowing gettering of surface regions, where the operational microelectronic devices are confined, by the precipitation of oxygen defects away from the wafer surfaces. A simple option for improving the suitability of CZ material for photovoltaics may be merely to change the crucible material used in the CZ process. For example, experiments have been conducted with silicon nitride coated crucibles as a way of reducing oxygen content within the material while increasing that of nitrogen (Shimura, 1989). However, relatively little exploration of such possibilities has been undertaken, probably because the benefits would not, in any case, be seen with the standard screen-printing approach. More sophisticated cell processing sequences would be required (such as offered by the buried-contact approach) to obtain the full benefits from such improved temperature tolerance. As opposed to the case of CZ silicon, much experimentation has been conducted with directionally solidified multicrystalline silicon. It may well be that multicrystalline silicon eventually exceeds the standard CZ material in its performance potential for photovoltaics due to the eventually better high temperature tolerance of the material. For example, the recent demonstration of 19.8% efficiency upon multicrystalline silicon (Zhao *et al.*, 1998) puts the performance of this material right in the middle of the performance range observed with a similar sequence using CZ wafers (Wettling *et al.*, 1996).

The trend towards thinner cells that arises primarily from efforts to reduce the costs of the silicon wafer may actually help to improve the cell efficiency. Thin wafers give the opportunity for back-surface fields or other rear-surface passivation approaches to be used to improve cell performance, primarily through increased voltage output. Again, the buried-contact processing sequence would be capable of realising such potential performance advantages due to its high open-circuit potential, which is largely untapped in wafers of standard thickness.

Bifacial cell designs offer another way of effectively improving cell efficiency. Recent studies suggest that module output can be improved by approximately 20% in standard open back configuration without any special effort if use can be made of light scattered onto the rear of the module (Chieng and Green, 1993). However, as cells are

now being increasingly used in the residential market where rear illumination of the module is unlikely, only part of the market would benefit from this improvement.

Japanese groups in particular are showing increasing interest in amorphous and microcrystalline silicon-based surface passivations as demonstrated by the 'HIT' cell structure (Tanaka, *et al.*, 1993; Sawada *et al.*, 1994), as shown in Fig. 4.15. This cell structure has demonstrated an open-circuit voltage capability similar to that of the buried-contact approach. However, it is inherently incapable of giving a similar current output due to light absorption in the 'transparent' conducting oxide layer required to give lateral conductivity to the amorphous silicon emitter as well as the less than 100% collection efficiency from the latter region.

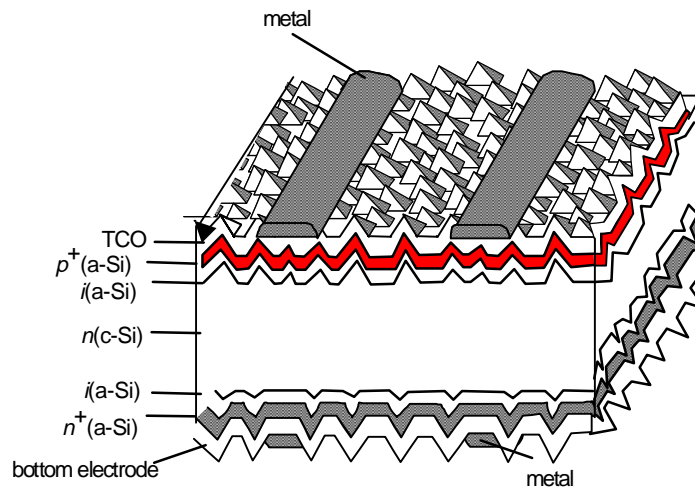


Figure 4.15 HIT (Heterojunction with Intrinsic Thin Layer) cell on textured crystalline silicon substrate. After Green and Hansen (1998).

Given better feedstock material or cells below 150 μm in thickness, improved rear-surface passivation approaches such as demonstrated by the PERC and PERL cells of Fig. 4.7 could become appropriate. A promising start has been made with the double sided buried-contact cell which applies high quality oxide passivation to both top and rear surfaces (Green, 1995). Other options may be rear passivation layers based on amorphous, microcrystalline or polycrystalline silicon (Okamoto *et al.*, 1997), or on specially deposited silicon nitride (Aberle *et al.*, 1997).

4.6.2 Laboratory cells

For laboratory cells, an appropriate reference point for performance is the AM1.5 detailed-balance efficiency limit of 33% for material of the band gap of silicon. However, it has been shown that another intrinsic process, Auger recombination, provides a more severe fundamental limit for silicon than the radiative recombination processes assumed in the detailed-balance limit (Green, 1984; Tiedje *et al.*, 1984). Unlike the detailed-balance limit, the Auger limit for a silicon cell is dependent on the cell thickness, as shown in Fig. 4.8 (Green, 1995). This difference arises because the detailed-balance calculation includes photon recycling which makes net recombination rates independent of cell volume. With lambertian light trapping, the optimum cell performance in the Auger limit is 29% for a cell of about 80 μm thickness. Such a cell would have an open-circuit voltage of about 760 mV, higher than the highest value ever demonstrated for silicon of 720 mV. The voltages of these best performing experimental devices demonstrating 720 mV were limited by surface recombination rather than bulk recombination. Figure 4.16 shows the results of efficiency calculations with various amounts of surface recombination added, characterised in terms of the open-circuit voltage limit that this recombination would impose if it were the only recombination process in the cell. Increasing surface recombination reduces the value of the obtainable efficiency as well as pushing the optimum cell thickness to larger values.

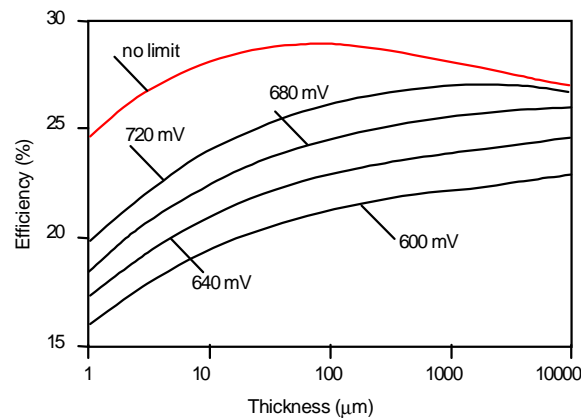


Figure 4.16 Limiting efficiency of silicon cell with lambertian light trapping as a function of surface recombination velocity, characterised in terms of the voltage limit imposed by this recombination. Source: Green (1999).

Figure 4.16 makes it clear that, to improve silicon cell efficiency much beyond 26%, improved surface passivation (both surfaces) is essential beyond the 720 mV capability presently demonstrated. If this improved quality cannot be achieved, an alternative possibility is to maintain the same quality of surface passivation as presently demonstrated and reduce the effective threshold energy of the photovoltaic process within the bulk regions of the cell. Techniques such as alloying sections of the cell with germanium to reduce its band gap (Healy and Green, 1992) or doping with a photoactive impurity to give impurity photovoltaic effects in the bulk region (Keevers and Green, 1994) have been suggested and shown, in some cases, to have theoretical advantages. However, no experimental performance advantage has been demonstrated by either technique to date.

A well-proven approach for improving solar cell efficiency is the use of the tandem cell structure. Efforts to produce tandem cells with silicon have not yet given good results due to the inability to find a suitable wide band-gap partner that is lattice-matched to silicon (Corkish, 1991). For low-quality cells, amorphous silicon/polycrystalline silicon tandems have given improved results over either cell type alone (Yamamoto *et al.*, 1997; Shah *et al.*, 1997). As the quality of the polycrystalline lower cell in this combination improves, however, it is doubted that this situation will continue (see Section 4.7). A higher performance top cell will eventually be required, which could be provided by a crystalline compound cell if difficulties with lattice mismatch to the silicon substrate can be overcome.

Fuller use of the available photon energy by incorporating efficient impact ionisation process has been suggested as a way of boosting cell performance by generating more than one electron-hole pair from one high energy photon (Kolodinski *et al.*, 1993; Werner *et al.*, 1994). However, such processes are quite weak in silicon with increases in current density limited to less than 0.1 mA cm^{-2} (Green, 1987). Manipulating the details of the band gap of silicon, for example by alloying with germanium, may improve prospects. However, since the high-energy photons of most interest for this process are absorbed very close to the surface of silicon, such approaches may interfere with the ability to obtain well-passivated surfaces. Limited experimental work with shallow germanium implants has not given any nett performance benefit (Keevers *et al.*, 1996).

More advanced concepts such as the multiple quantum wells discussed in Ch. 10 might also be appropriate (Barnham and Duggan, 1990). A recent area of interest has been the use of ZnS/Si multiple quantum wells. Not only is there a good lattice match between ZnS and Si, but recent studies suggest it may be easier to obtain direct band-gap-like properties from such multiple quantum wells than the Si/Ge alternative which has been the focus of most past study. There is still some question as to whether or not

a multiple quantum well device offers a performance advantage above the detailed-balance limit (Araujo *et al.*, 1994), but this approach almost certainly offers performance advantage above the Auger limit for silicon, in principle.

4.7 Silicon-supported thin films

There has long been an interest in transferring the strengths demonstrated by crystalline silicon wafer technology to cells based on silicon thin films. Historically, work can be divided into two phases: (i) that before the 1980s when the benefits of light trapping were not fully appreciated; and (ii) that after the mid-1980s where light trapping has been regarded as an essential feature of any silicon thin-film cell design. The early work laboured under what is now known to be a misconception that quite thick layers ($>20\text{ }\mu\text{m}$) of silicon would be required to give reasonable performance due to silicon's poor absorption characteristics arising from its indirect band gap (see Fig. 4.8). However, since light trapping can increase the effective optical thickness of a silicon cell by 10–50 times, this means that layers of only $1\text{ }\mu\text{m}$ or so thickness are still inherently capable of producing similar performance to much thicker layers.

Approaches to producing supported silicon films can be divided into high-temperature and low-temperature strategies depending on whether or not the substrate is heated to high temperature during the silicon deposition or subsequent processing.

4.7.1 High-temperature supported films

One of the earliest silicon supported film approaches was the 'silicon-on-ceramic' approach (Christensen, 1985) whereby a ribbon of ceramic material was dipped into a molten silicon bath or pulled across the surface of a silicon melt so that one side was coated with silicon. This produced silicon of modest quality and the approach suffered from difficulties in making rear contact to the cells, since the ceramics used were insulating. This approach was discontinued in the early 1980s. Early work by Ting and Shirley Chu involved the deposition of silicon onto a range of foreign substrates by high temperature chemical vapour deposition (Chu, 1977). Operational cells were obtained using a number of substrate materials. The best results were obtained by depositing the silicon layers on multicrystalline silicon substrates prepared from metallurgical grade silicon. Given the previous studies that have shown that sawing of wafers represents one of the major costs in any wafer-type approach, the overall economics of such an approach using a wafer substrate are questionable, regardless of

the quality of this substrate. Other early work involved the deposition of silicon onto ceramic substrates by high temperature CVD and the subsequent increase in crystal size by melting and directional solidification (Minagawa *et al.*, 1976).

In the post-1980 era, efforts in silicon supported film were revitalised by the US company AstroPower (Barnett *et al.*, 1985). In this company's approach, silicon is deposited onto a conducting ceramic substrate by a technique which has not been disclosed but which has been reported to involve the deposition of silicon from solution in molten metal as one step (Barnett *et al.*, 1989). The resulting ceramic-based wafers can then be processed in the same way as a multicrystalline silicon wafer. Efficiency up to 16.6% has been confirmed for films that are apparently in the 50–100 μm thickness range (Bai *et al.*, 1997). Efforts are underway to include more effective light trapping into these devices and to produce an integrated module upon insulating ceramic (Ford *et al.*, 1997).

More recently, promising laboratory results have also been obtained by a German collaborative effort using much thinner films. These films were formed by first depositing and recrystallising a thin silicon layer upon a silicon carbide coated graphite substrate followed by the deposition of an epitaxial layer of silicon of about 30 μm thickness upon this recrystallised layer. Cell efficiency above 11% has been confirmed for a cell of this 30 μm thickness (Lüdemann *et al.*, 1997).

4.7.2 Low-temperature approaches

One of the first papers addressing silicon photovoltaic thin films described the deposition of silicon by low temperature chemical vapour deposition onto an aluminium substrate (Fang *et al.*, 1974). A surprisingly large grain size was obtained, attributed to eutectic reaction with the aluminium. In more recent times, laser crystallisation has been used in the active matrix liquid crystal display industry to produce relatively small-grain polycrystalline silicon films from amorphous silicon precursors, generally deposited by low-pressure chemical vapour deposition. Grain sizes are typically less than a micron or so, so that these films would probably not be suitable for photovoltaics. Also, thicknesses for the active matrix display industry tend to be only about 100 nm, which would be too thin for photovoltaic application.

From 1989, a group at Sanyo explored the use of low-temperature solid-phase crystallisation of amorphous silicon as a technique for producing thin-film polycrystalline silicon cells. Good results have been obtained with 9.2% (unconfirmed) efficiency reported in 1995 (Baba *et al.*, 1995). These cells were approximately 1 cm^2 in area deposited onto a textured metallic substrate and heated at

approximately 600 C for many hours to enable the crystallisation of the originally amorphous films. After crystallisation, the HIT structure developed by Sanyo is used to complete the cell processing at low temperature.

Two groups have reported good results using silicon thin films deposited directly in microcrystalline form onto glass substrates. The University of Neuchatel has reported unconfirmed efficiencies of about 7% for 3 μm thick microcrystalline cells deposited at 500 C (Shah *et al.*, 1997). The cell has a *p-i-n* structure with the intrinsic region comprising most of the device thickness. The cell is designed for this intrinsic region to be depleted during normal device operation to create a high electric field to aid carrier collection, as with a standard amorphous silicon cell. Finally, Kaneka Corporation (Yamamoto *et al.*, 1997) has reported efficiencies over 10% with a similar device structure, shown in Fig. 4.17. Nearly the same efficiency was obtained when the total device thickness was varied over the 1.5–3.5 μm range. Both the above groups have reported even higher efficiencies when amorphous silicon cells are used in a tandem configuration on top of the microcrystalline device. Given the relatively small amount of effort so far dedicated to this area, these results are extremely encouraging, and show the enormous potential of such low temperature approaches.

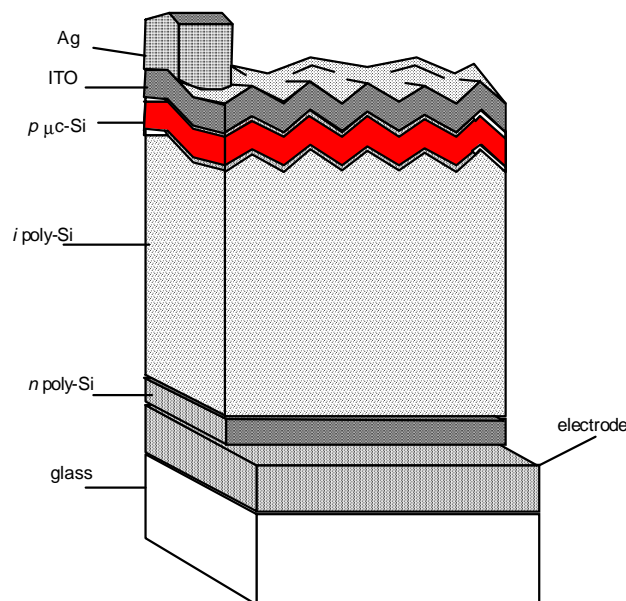


Figure 4.17 Structure of 9.4% efficient thin-film microcrystalline solar cell developed by Kaneka. Cell thickness is typically 1–3 μm . After Yamamoto *et al.* (1997).

4.7.3 Multilayer solar cells

The parallel multilayer solar cell shown in Fig. 4.18 provides an effective cell design when dealing with low quality silicon such as obtained by low temperature approaches (Green and Wenham, 1994). This cell differs from a tandem cell because all junctions are connected in parallel. The active region of any cell is the depletion region straddling the metallurgical junction and the region within a diffusion length on either side of this depletion region. The challenge in producing a thin supported silicon device of high performance is therefore in having material quality sufficiently good for this active volume to be wide enough to result in a large amount of current collection. In the microcrystalline work previously reported, attempts have been made to enlarge this active region by expanding the junction region by making this region as lightly doped as possible. The multilayer approach provides an alternative (or complementary) way of achieving the same result. By having multiple p - n junctions dispersed throughout the material, it is possible to make the whole volume of material electronically active regardless of material quality. The approach is particularly appropriate when the parallel layers are very heavily doped allowing unique thin-film cell and module designs where the lateral conductivities of the doped layers are sufficiently high to allow lateral current flow without appreciable resistance loss. This removes the need for transparent conducting oxides used in other thin-film technologies to provide this lateral conductance.

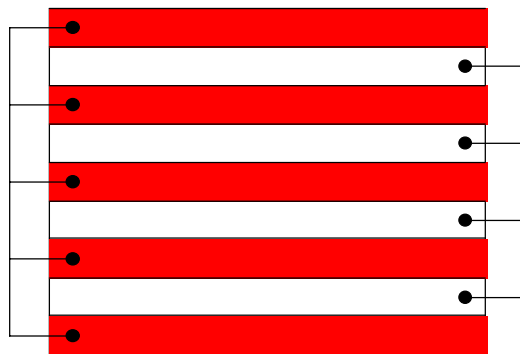


Figure 4.18 Parallel multilayer cell schematic. The red and white layers correspond to different doping polarities. Each layer is thinner than the minority carrier collection distance. Source: Green and Hansen (1998).

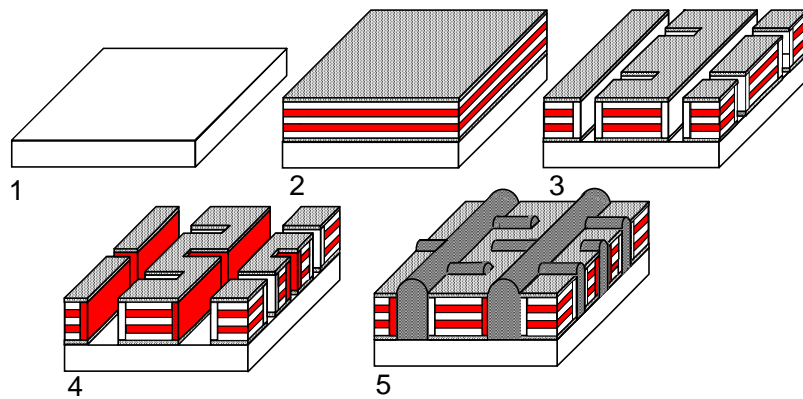


Figure 4.19 Fabrication of UNSW multilayer cells: 1. Glass superstrate; 2. Multilayer deposition; 3. First polarity groove; 4. Second polarity groove; 5. Metallisation. The cell is designed to be illuminated from the glass side (the underside in this schematic) although bifacial operation is feasible. Opposite polarity regions in adjacent cells are connected, providing automatic series connection within the module. Source: Green and Hansen (1998).

At UNSW, the parallel multijunction approach has been combined with the buried-contact approach to produce the device fabrication sequence shown in Fig. 4.19. After deposition of a multilayer stack on a low temperature substrate such as glass, laser grooving and groove doping of one polarity is applied to connect all the layers of this polarity together in parallel. A second laser grooving and doping step involving the other polarity follows. By aligning to the first step, series interconnection of the cells is also achieved in a very elegant process. Pacific Solar in Sydney is working on commercialising this process, although few details have yet been published (Pacific Solar, 1997).

4.8 Summary

Although crystalline silicon devices have dominated the commercial marketplace for photovoltaics for more than two decades, there still remains scope for considerable improvement in both the performance and cost of these cells. Recent studies suggest that manufacturing costs well below US\$1/W_p are obtainable in manufacturing volumes of 500 MW_p per year, without major changes in present processing sequences. This suggests module costs will steadily decrease from present values of about US\$4/W_p as manufacturing volumes continue to increase. The average energy

conversion efficiency of product sold should also increase due largely to the increasing market share of high efficiency approaches, particularly the buried-contact cell approach. The trend towards thinner silicon wafers to decrease wafer cost is compatible with ongoing increases in cell efficiency provided cell structures as effective as the buried-contact approach are adopted and improved methods are demonstrated in production for passivating the rear surface of the cell. Substrates with more consistent high temperature performance than standard CZ grown silicon may be required to allow the full performance potential of the silicon wafer approach to be obtained. Particularly promising progress has been made in this area with multicrystalline silicon over recent years. This enormous potential for both performance and cost reduction will make these bulk silicon approaches an increasingly challenging target for the thin-film approaches currently under development. In this context, excellent recent progress has been made with supported silicon film. Films processed at low temperature on substrates such as glass have made exceptional gains in the laboratory over the last 2–3 years and offer great promise for stable low cost thin-film cell technology for the future. Innovative cell design such as the parallel multilayer cell will allow the particular properties of thin-film silicon to be used to their full advantage.

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