PILOT-LINE CIGSSE POWER MODULE PROCESSING AND QUALIFICATION AT SHELL SOLAR

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ABSTRACT: Objective of the Shell Solar CIS thin film development is a high performance, high quality module product to be processed in a profitable production line. At the Shell Solar central R&D facility in Munich we develop the 2nd generation CIS modules on 30x30 cm^2 and 60x90 cm^2 substrate formats. The key features are sputter deposition of a Cu-In-Ga-Se precursor, controlled sodium doping and rapid thermal processing (RTP) in a sulfur containing ambient, sputter ZnO window layers and a low-cost frameless module package. For process control at an early stage in-line metrology tools such as photoluminescence lifetime measurements, Raman spectroscopy, and infrared thermography have been implemented in the pilot line. Aperture area efficiency of 30 x 30 cm^2 standard pilot line circuits is 12.3% with tight distribution and peak module efficiencies of 13.4%. We recently started routine processing of 60 x 90 cm^2 modules. The aperture area efficiencies of the 60x90 line average at 12.5% resulting in a total average output power of 60 W_p per module. A first 1.4 kW array was installed on the Munich-site for the evaluation of outdoor performance. Reliability, durability and climate stability of our frame-less glass-glass package is demonstrated following the IEC 61646 protocol, i.e. damp-heat, thermal cycling, humidity-freeze, insulation, wet leakage current, wind load and insulation testing. Aiming at the replacement of Cd from product and production two approaches are developed: a) Chemical bath deposition of Zn(S,OH) compound layers yields 13.2% efficiency on cells and 10.5% on 30x30 cm^2 modules. b) Using (Zn,Mg)O sputter deposition, thereby omitting wet-chemical processes, efficiencies of 11.7% (cell) and 9.1% (30x30% module) have been achieved so far.
Keywords: Thin film solar cells, chalcopyrite, CIS, ZnO

1 INTRODUCTION

Thin film modules based on the chalcopyrite family (e.g. $CuInSe_2$, CIS) have reached a high performance level in pilot manufacturing lines with annual production capacities that range from a few kW to MW [1-5]. Further scale-up of production volumes has been slower than initially expected though: higher volume and high yield production equipment for the multi-component absorber materials and the monolithic cell integration had to be developed, constructed and steadily improved together with equipment developers and suppliers. We have recently scaled-up our second generation CIS process to the substrate size of 60 x 90cm^2. This process addresses manufacturing issues like in-line process capability as well as the decoupling of key processes in the absorber formation: Na dosing, film deposition and crystal growth. While fundamental investigations are still required for the understanding of the absorber formation process, as well as the creation and physics of the hetero-interface, the focus in the pilot lines shifts to process control, yield issues and the design of the appropriate package. For a better process control we have developed process control tools tailored to the needs of CIS technology. Climate stability, reliability and durability of the modules, as a future product on the market, become equally important as efficiency. They are tested by accelerated stress tests according to internal design qualification and type approval following IEC 61646, i.e. damp-heat, thermal cycling, humidity-freeze, insulation and wet leakage current testing. In this paper we will present recent performance data of our pilot line and report on the result of the module qualification tests.

Cadmium-free buffer layers are expected to increase the market acceptance of CIGSSe devices. In addition, more begnin buffer layers would simplify the health and safety requirements in production and reduce the amount of waste, both reducing the production costs for such thin film devices. We will present recent results of various approaches.

2 PILOT LINE PROCESS

2.1 Process description

Our core process of CIS absorber formation, denoted SEL-RTP process (rapid thermal processing of stacked elemental layers), has been presented previously in detail [6], [7], [8]. The full process sequence is illustrated in Fig. 1. In order to achieve low-cost thin film modules float glass substrates are used. For reproducibility in substrate surface conditions and in alkali doping, silicon nitride is deposited as an alkali-barrier layer on top of the float glass surface. Controlled sodium doping is a key feature of the SEL-RTP-process: the application of a barrier layer enables a well-defined Na dosage prior to the absorber formation process. The deposition of all precursor layers is performed in a modified vertical in-line sputter coater. The back electrode (Mo), the Na dopant compound and several alternating layers of Cu(75%)+Ga(25%) and In are deposited by DC magnetron sputtering. The Se layer is deposited on top by thermal evaporation through a linear source. Selenization and sulfurization is performed in a custom built large area RTP reactor. Sulfurization is performed by adding a sulfur containing gas into the reaction chamber. The CdS buffer layer is deposited by a chemical bath deposition process using the decomposition of Thiourea.

The ZnO deposition is performed in a commercial glass coater using magnetron sputtering from ceramic targets. The patterning of Mo (P1) uses a pulsed laser operating in the near-infrared. Mechanical scribing is applied for patterning of absorber (P2) and ZnO (P3). Before lamination of a coverglass to the circuit substrate thin film edge deletion and contacting are performed. All

process steps from substrate wash to lamination can now be performed on 60x90 cm^2 substrates. The 60x90 cm^2 module is designed to be used (and is tested) without a frame. If required for some application framed versions would of course also be feasible.

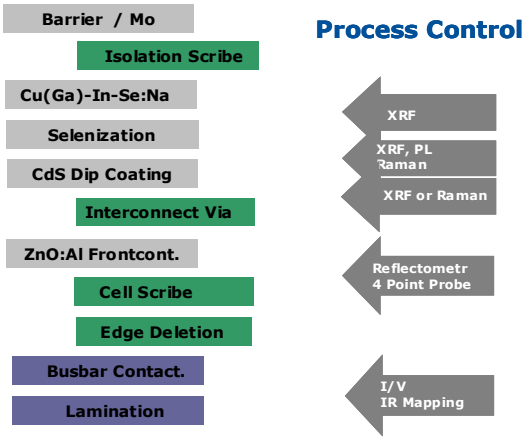


Figure 1: Process scheme for CIGS-modules with monolithic integration of series connected cells. The arrows indicate process control steps.

2.2 Process control tools

In contrast to silicon PV technology the CIS module contains only one monolithic circuit that has accumulated a considerable amount of material and process value before it can be I-V tested. Process control tools allow for a control of material parameters like film thickness, composition, or minority carrier lifetimes at an early stage of the process. Figure 1 displays the process control tools that are developed for the second-generation process [8]. Precursor thickness and composition are determined by X-ray fluorescence. In the pilot-line we still use a wavelength dispersive analytical system that allows for determining moles and mole fractions of all constituents and films from Na to Zn on small (3x3 cm^2) samples. Large substrate area and high volumes in a production environment preclude the use of wavelength dispersive systems. Commercial energy dispersive systems are, instead, available for large substrates and for in-line systems. The energy resolution of these systems is sufficient to measure Cu, In, Ga and Se without the need of vacuum chambers. After absorber formation the anion stoichiometry ratio S/Se, however cannot be reliably determined by energy-dispersive systems, as the Mo-L and the S-K lines cannot be resolved. We therefore developed Raman spectroscopy as a contactless, nondestructive tool for the detection of the S/Se ratio [9]. A separate paper at this conference describes the application of Raman for the measurement of microscopic and macroscopic variations of S/Se, for the detection of secondary phases in growth experiments and for the measurement of the CdS buffer thickness [10]. In order to monitor the electronic quality of the absorber we measure the minority carrier lifetime by using photoluminescence (PL) decay at room temperature. For process control we integrated a custom built spectrometer into an x-y stage for the automated measurement of 30x30 cm^2 CIS absorbers [11], [12]. The CdS buffer layer thickness currently is monitored by XRF, but Raman spectroscopy may replace it in a production line.

The ZnO properties are determined by interferometric measurement of the thickness and by four-point probe for the sheet resistance. After I-V testing we use infra-red thermography for failure analysis. This technique uses an IR camera triggered by an external bias voltage pulse and records the local temperature increase within a large PV device as a result of resistive losses or due to microshunts [13]. Particularly the patterning process can be characterized by this technique.

3 PILOTLINE PERFORMANCE

3.1 Substrate size of 30x30 cm^2

The 30x30 pilot line is the working horse of our large area development work: while precursor deposition and RTP process were scaled up to 60x90 cm^2 since 2001, all back end process had to be performed on 30x30cm^2 up to 2004. The progress in large area selenization can therefore be best compared by comparing 30x30 line results, see Fig 2. In 2002 we reported on the first 30x30 efficiencies with average efficiency of 10.6% [14]. Figure 3 demonstrates the excellent performance of the present pilot line: the average circuit aperture area efficiency is now at 12.3% with a standard deviation of 0.3%. The histogram compiles the data of 120 circuits. Not all circuits are processed into modules. The best module has reached 13.4% due to reduced reflection with a laminated front glass.

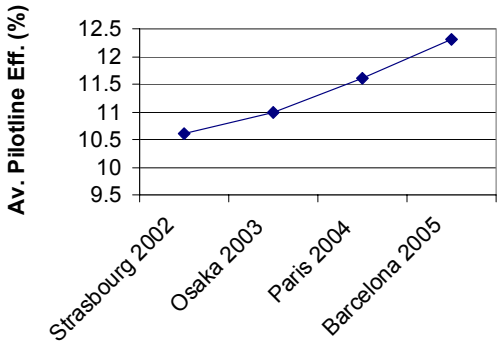


Figure 2: Progress of Efficiency of Munich Pilotline: Strasbourg 2002 [14], Osaka 2003 [15], Paris 2004 [1], Barcelona 2005: this conference.

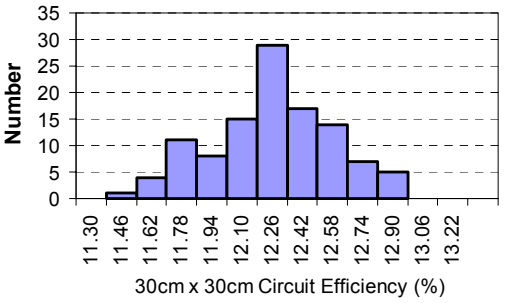


Figure 3: Efficiency Distribution of 30x30 cm^2 circuits.

3.2 Substrate size of 60x90 cm^2

In fall 2003 we presented the first 60x90cm^2 module that was manufactured in cooperation with the CIS production line in Camarillo [15]. While absorber formation was performed in Munich with the SEL-RTP process the CdS buffer and the MO-CVD ZnO front electrode was deposited in Camarillo. With only a few parts processed we had achieved a record efficiency of 13.1% (65W). In 2004 we began to scale up the back end processes CdS buffer deposition, ZnO sputter deposition, edge deletion, and contacting to 60x90 cm^2 substrate size. Figure 4 presents the efficiency distribution of the now completed 60x90 cm^2 line. The histogram shows that the most frequent value of 12.3 % is exactly at the average of the 30x30 line while the 60x90 average is even slightly higher at 12.5% with equally narrow distribution. This result demonstrates the excellent lateral homogeneity and stability of all processes including the RTP absorber formation.

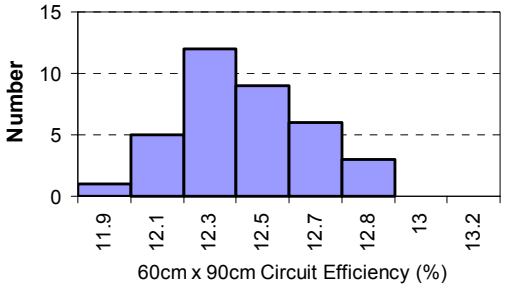


Figure 4:Efficiency Distribution of 60x90 cm^2 circuits.

3.3 Outdoor test array of 1.4 kW

A set of 24 modules of 60x90cm^2 size was manufactured for a solar roofing system. The modules were designed as shinglesthe modules overlap with the upper top edge. . Figure 5 shows a photograph of the outdoor array that was installed at the Munich R&D facility site. The average aperture area efficiency was 12.4% resulting in a total area module efficiency of 11.1% and a total power of 60W$_p$ per module. The total installed power hence was 1440W. Figure 6 shows the daily yield and the cumulative yield of May 2005 normalized to initial power measured indoor under standard testing conditions (STC). The plot also contains the respective values of an array of Shell Solar monocrystalline Siliconmodules with 165W. The normalized yield and cumulated yield curves of the CIS modules are comparable or even slightly above the silicon references. In Figure 7 the normalized power is plotted for both arrays for the sunniest and the darkest day in May. Again, both curves mostly coincide with a slight advantage for the CIS prototypes. Note that with a total area module efficiency of above 12.5% the absolute power per m^2 array is still higher for mono Silicon modules but in the meantime approaches most multi-crystalline Si modules.

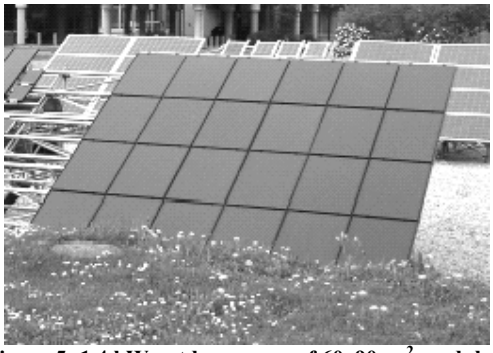
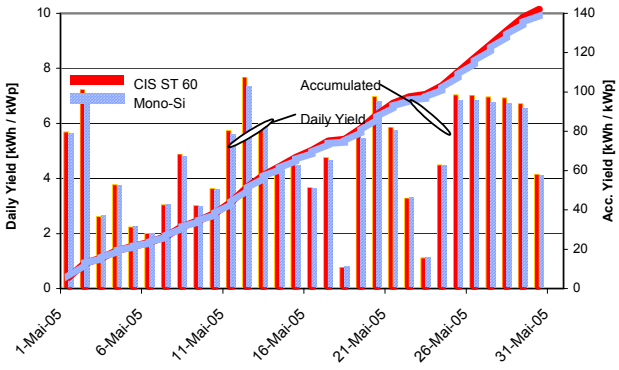


Figure 5: 1.4 kW outdoor array of 60x90cm^2 modules

Figure 6: Daily and cumulative power yield normalized to initial indoor measurement at STC for the Pilotline



outdoor array and a Silicon module reference array.

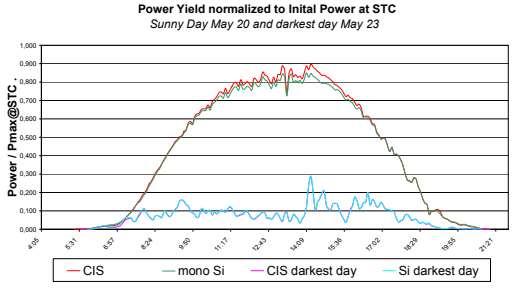


Figure 7: Power normalized to initial indoor measurement at STC for the Pilotline outdoor array and a Silicon module reference array for the sunniest and the darkest day in May 2005.

4 ACCELARATED STRESS TESTS

4.1 Tests on 30x30 cm^{2}Modules

We previously reported that two 30x30cm^2 pilotline modules have successfully passed the damp heat branch of the IEC 61646 [15]. The test was carried out and the result was certified by the external test centre TUEV Immissionsschutz und Energiesysteme, Germany. With every circuit and module improvement step we perform the same test in-house. Figure 8 shows the result of a set of modules of the state of end of 2004 starting with an aperture area efficiency of 11.7%. Beforehand the

modules were power stabilized by two successive annealing cycles (subject to the regulations of IEC 61646, test 10.19). No test sample showed major visual defects after the test. After 1000 hours of damp heat according to test 10.13 of IEC 61646 the power loss was slightly less than 5% compared to the initial stabilized values. After 30 min of additional light soaking at 1 sun the power loss compared to the initial stabilized values amounted to 3%. These values are within the acceptance limit of –5% given by IEC 61646. An additional set of modules was subjected to the insulation test, the wet leakage test before and after damp heat, as well as the thermal cycling and humidity freeze test according the IEC 61646 standard. All tests were successfully passed.

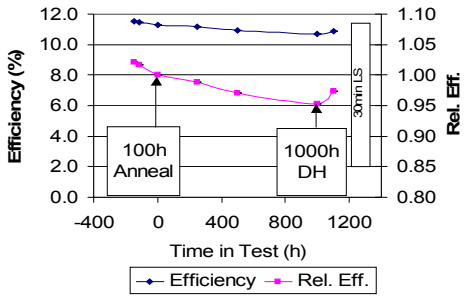


Figure 8: Pilotline modules (30x30cm²) pass damp heat test according to IEC 61646 with low cost glass glass package. Left axis efficiency, right axis relative efficiency normalized to annealed state.

4.2 Tests on 60x90cm^2 Modules

For the latest generation of 30x30cm^2 as well as the 60x90 cm^2 the accelerated climate testing is still on-going. The 60x90 cm^2 module package is very similar to the 30x30cm^2 design. We therefore began with the most critical size related test, the wind load test. As long as device processing was not ready we started testing of dummy modules. In order to account for possible thermal stress during processing we processed Mo covered substrates through RTP, applied edge deletion and attached the bus bars. The dummies were laminated to a 4mm front glass. The frameless design tolerated loads of 4kPa and more without breakage. The wet leakage test was passed, too, before and after damp heat testing.

5 CD-FREE BUFFER LAYER

In order to omit the CdS buffer layer from the device we investigated two potential alternatives: First, a Zn(S,OH) compound buffer deposited by chemical bath deposition (CBD), i.e. using the same deposition equipment as for the CdS buffer layer [3], [16]. Second, a (Zn,Mg)O layer replacing both CdS and i-ZnO layer, deposited by RF sputtering from a mixed oxide target [17], [18]. Here, a wet-chemical step - from the view-point of an in-line production undesired – might be completely omitted and only standard sputtering equipment be used.

5.1 Zn(S,OH) buffer layer

We use a chemical bath consisting of zinc acetate, ammonia, and thiourea to deposit a thin Zn(S,OH) compound layer [3], [16]. As this process is based on a cluster-by-cluster growth mechanism, the new process needs a much tighter control than the corresponding CdS process which is known to be dominated by an ion-by-ion growth mechanism. The depositions are done in a custom made CBD equipment at 80°C while continuously filtering the solution and applying ultrasonic agitation of the bath. Such processing helps to prevent Zn(S,OH) agglomerates from incorporation in or onto the growing film, so that a more uniform coating of the CIGSSe absorber is reached. The CBD process is followed by vacuum annealing of the devices, to transform zinc hydroxide species into zinc oxide.

Such buffer layers have to be essentially thin (<10 nm), but still uniform to reach sufficiently good band alignment between absorber and window. Therefore, the deposition process is under on-going investigation. Best cell efficiency reached so far is 13.2% (1.4 cm² active area), and the best 30x30 cm² module has an efficiency of 10.5% (see Fig. 9). Such glass-glass laminates have been tested under damp-heat conditions according to IEC 61646 and passed the test criteria.

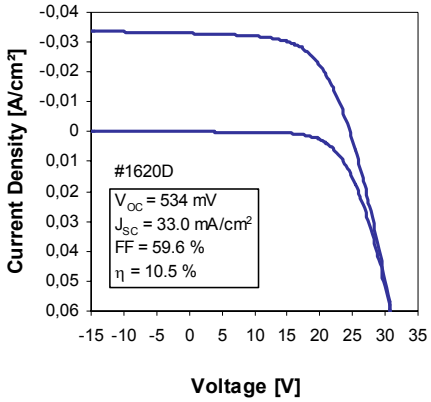


Figure 9: IU data for the best Zn(S,OH) buffered CIGSSe module (aperture area 727.3 cm²)

5.2 (Zn,Mg)O layer

The (Zn,Mg)O layers were RF-sputtered from a mixed-oxide target containing 15at% Mg. With this target, reproducible layers could be deposited, while a previously used target with 30at% Mg proved unstable over time. So far, the best devices with a completely dry (Zn,Mg)O buffer layer reach 11.7% efficiency for a 1.4cm² test cell and 9.1% for a 30x30cm² glass-glass laminated module. Here, optimization focuses on the sputter deposition conditions and absorber surface chemistry.

6 SUMMARY AND OUTLOOK

We presented the current status of the pilotline of our second generation CIS process. The 30x30 cm^2 line aperture area circuit efficiency averages now at 12.3% with a narrow distribution of 0.3% standard deviation. The best module reached 13.4%. The recently completed 60x90cm^2 line demonstrates the excellent lateral homogeneity of our processes as the average efficiency

and distribution are equal or even slightly better compared to the 30x30 cm^2 line. Process control tools like XRF, Raman spectroscopy, photoluminescence lifetime measurements and infrared thermography play a key role both in the process development and the maintenance of a stable process with low variance. We also built a first 1.4 kW outdoor array. The presented performance data shows high power yields with respect to the initial indoor measurement at standard test conditions. We reported that our 30x30 cm^2 modules passed several accelerated stress test (in-house) according to IEC 61646 including the damp heat. The qualification of our 60x90cm^2 is still ongoing. The first tests show good mechanical stability of our frame-less module design. We will continue the further qualification of our 60x90 cm^2 prototype design according to IEC 61646 and safety class II regulations. We outlined two approaches to Cd-free buffer layers; CBD Zn(S,OH) and sputter (Zn,Mg)O. The best 30x30cm^2 module with a CBD Zn(S,OH) buffer and sputter ZnO reached an efficiency of 10.5%. We will now focus on the efficiency improvement of Cd-free buffer layers.

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