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CMP for Metal-gate Integration p. 14

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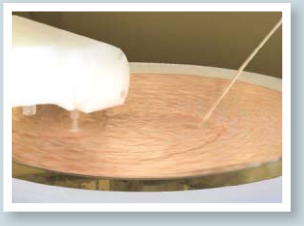

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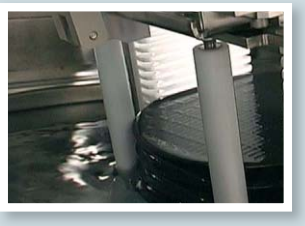

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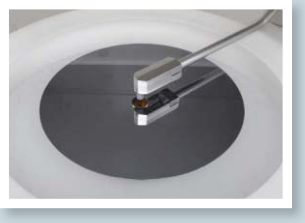

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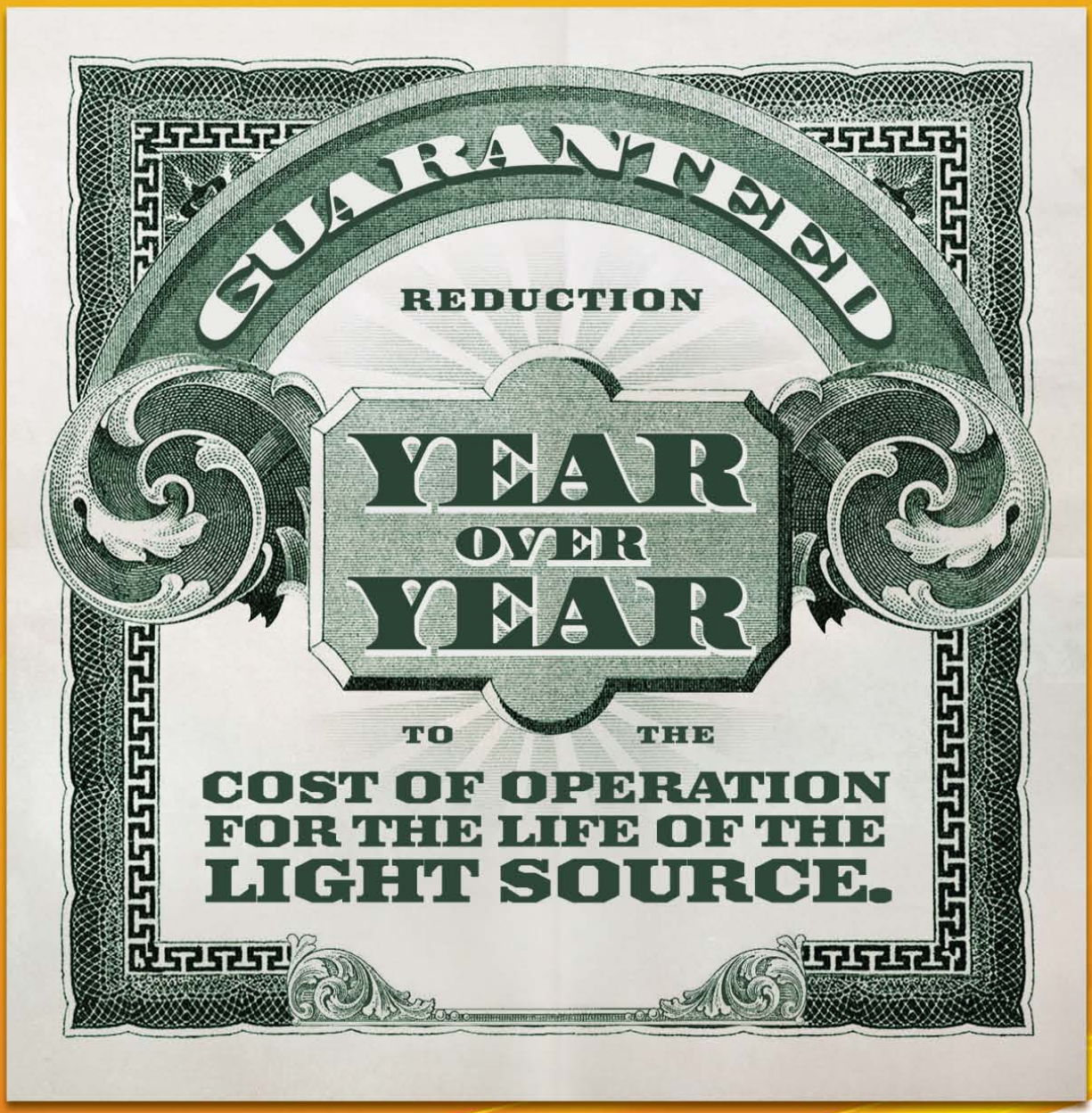

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Advanced Packaging

NOVEMBER 2010 Vol. 53 • No. 10

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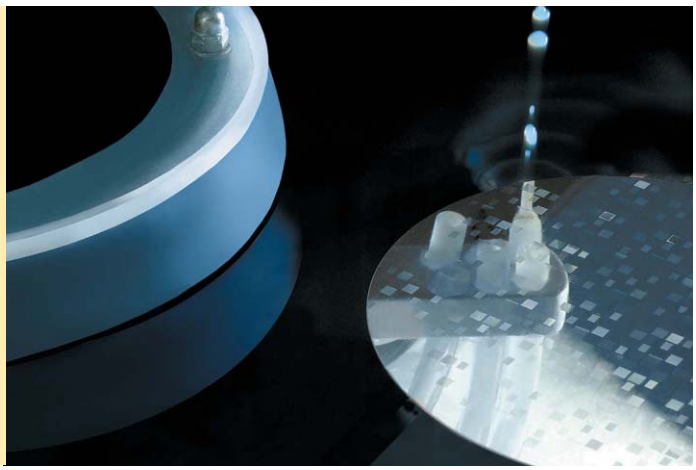
The methodical tuning of slurry additives provides for the successful integration of both poly-open and Al CMP into HKMG process flows. Source: Cabot Microelectronics Corp.



FEATURES

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Podcasts: Techcon, MEPTEC, Freescale

SST's Debra Vogler spoke with organizers and presenters at the Semiconductor Research Corp.'s annual TECHCON research meeting, including work on Cu/low-*k* extendibility and CMOS-MEMS integration. Also: analysts at a MEPTEC luncheon offer their forecasts, and Freescale's Bryce Osoinach discusses the company's new accelerometers. Check them all out *www.electroiq.com/podcasts*.

Shaping the photomask industry's structure

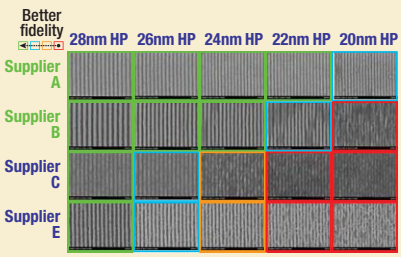
Using Michael Porter's "5 competitive forces that shape strategy" as a template, Franklin Kalk from Toppan Photomask examines the photomask industry: the threat of new entrants, the bargaining power of suppliers and customers, future products that could replace photomasks, and rivalry among existing lithography firms.

3D ICs on the roadmap

Advanced Packaging contributing editor Phil Garrou drills down into what the *ITRS* Roadmap's 2009 version says about 3D ICs and related topics in its sections on interconnects and assembly and packaging. Meanwhile, the recent SEMICON Taiwan 3D Technology Forum shed some insight into what several foundries, assembly houses, and customers are thinking about the timing for 3D interposers and full 3D IC.

Litho materials infrastructure from a collaborative research approach

Warren Montgomery and Stefan Wurm detail how SEMATECH's toolset and collaborative approach is keeping lithography moving forward by bridging the lapse between basic research and wafer fab production processes.

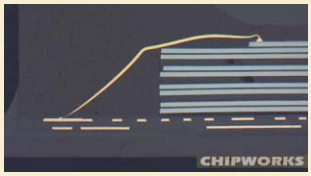


Wet cleaning improvements for Si surface preparation

Simple but effective enhancements to wet clean steps can help achieve more stringent surface preparation and reduce complexity, cost-of-ownership, and environmental concerns, writes Robert Pagliaro from RP Innovative Engineering Solutions.

Samsung's eight-stack flash shows up in Apple's iPhone 4

Chipworks' Dick James peers into the newest iPhone to see how the industry is pushing today's packaging options (wire bonds and ultrathin dies), and what it means for future use of through-silicon vias (TSV).



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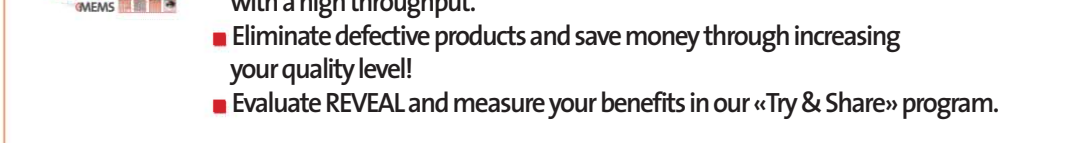

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EDITORIAL

The Grid Wants YOU!

Supply voltages, transmission losses, long-term reliability, IEEE standards, circuit simulations – those are familiar topics for those working in the semiconductor industry. But they are of equally high interest to another group: those working to improve the electricity grid.

Certainly everyone has heard by now that "The Grid," at least in the U.S., is fairly antiquated. DOE Secretary Stephen Chu recently quipped that if Thomas Edison were to suddenly come back to life he'd have no idea how an iphone works, but he'd be quite familiar with all the elements of the electricity grid. They've hardly changed since Edison designed the first grid for New York city more than 100 years ago.

Certainly many people – perhaps too many – have left the semiconductor industry to pursue a career in the exciting world of photovoltaics, where the substrate is usually silicon and the processes of doping, annealing, metallization and packaging are familiar. The output of the device, however, is not processed signals, but raw power.

What needs to happen to get the utilities to work together is simple: standardization. This is where those in the semiconductor industry can make an impact.

The world has embraced photovoltaics and other renewable energy sources such as wind, hydro, biomass and geothermal. One of the concerns moving forward is that the best of these sources – PV and wind – are inherently intermittent. Proponents of PV like to point out that although PV is intermittent (due to clouds and of course darkness), it's actually highly predictable. Clouds don't cause that much variability if the PV is spread out over a wide enough area, and because they are visible, it's relatively straightforward to predict the impact on power generation on a short-term basis and even easier to predict the amount of power that will be generated the next day based on weather reports. That's fine because power markets operate on a day to day basis.

One way to balance out that intermittency is through energy storage. Analysts see a strong, upcoming demand for energy storage as part of the grid. This will likely be a combination of some kind of central storage (i.e., a 20MW flywheel installation near a power generation station) and distributed storage (i.e., batteries next to the familiar green transformers in people's yards). These types of energy storage are primarily driven by a need on the part of utilities for load balancing, since it's expensive for them to constantly adjust the output of traditional power generation systems as the load varies. Energy storage may even allow them to offset or delay the requirement of additional power plants, such as a gas-fired "peaker" plants which are notoriously expensive.

In some markets, there is also value for companies and people on "the other side of the meter" to buy and store power when it is least expensive, and use the stored power during peak demand when prices are highest. Electric vehicles will also come into play, in part by helping to advance battery technology, but also by actually becoming part of the smart grid. Andy Chu, director of marketing at A123 Systems (Watertown, MA) envisions a time when utilities are so linked into the grid that they can monitor and control electric vehicle battery chargers during the night, and charge them quickly or slowly so as to optimize the load/generation equation.

This vision of the smart grid with renewable sources and energy storage working in harmony is complicated. The U.S. electric industry includes over 3,100 electric utilities. Investor owned utilities are privately-owned, represent 8% of the total, approximately 75% of generation capability and revenue. There are 2,009 municipal utilities, supplying approximately 10% of the generating capability and 15% of retail revenue. There are 912 cooperatives, operating in 47 States, accounting for 9% of total revenue and around 4% of generation.

What needs to happen to get them to work together is simple: standardization. This is where I believe those in the semiconductor industry can make an impact -- volunteering to participate in standards committees. One standard of importance is IEEE P1547.8, which is focused on high-penetration, grid-connected photovoltaic technology. Among the issues being discussed: active voltage regulation, voltage and frequency ride-through, frequency trip settings (under/over voltage), operation under fault conditions, switching, power quality, monitoring and control, and dynamically controlled inverters. Getting involved is easy: check out http://www.nrel.gov/eis/high_penetration_pv_wkshp_2010.html for more information. Your experience is needed! ■

Pete Singer
Editor-in-Chief

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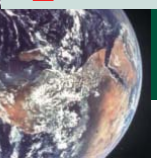


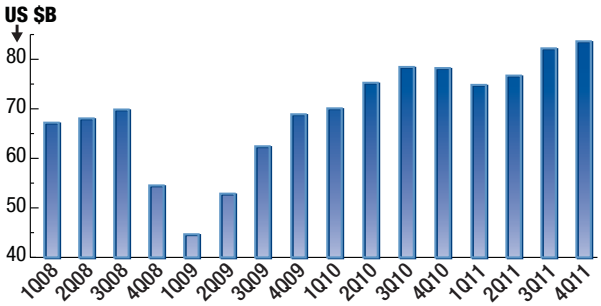
WORLD NEWS

BUSINESS TRENDS

Soft demand, inventories cause forecast rethink

Among the first semiconductor industry watchers to shift direction and lower their optimistic forecasts, iSuppli is trimming its 2010 chip sales forecast (to 32% from 35%), citing "a significant slowdown" in consumer demand for some electronic devices, including market bellwether PCs, even as inventories build throughout the supply chain. iSuppli SVP Dale Ford sees a slight decline (-0.3%) in semiconductor revenue growth in 4Q10, and 7.8% for 2H10 vs. 1H10, down from the 10.7% in 1H10 vs. 2H09.

But that doesn't mean the market has peaked and is heading down, Ford noted. Visibility is poor and uncertainty high due to unstable economic conditions and market reports, which has led to handwringing about a possible "double-dip" scenario for electronics and the overall economy. Instead, Ford sees a "soft landing in 2011" and not "the kind of dramatic downturn seen in 2009." He currently projects 5.1% growth in 2011 (vs. 7% in the previous forecast), with quarterly data points returning to more normal seasonal patterns: decline in 1Q, improvements in 2Q and a peak in 3Q.



WORLDWIDE HIGHLIGHTS

The Israeli government has approved an eight-year, up to 678M shekel ($187M) grant to **Intel** (vs. the $400M for which the chipmaker had lobbied) to help upgrade its Fab 28 in Kiryat Gat to 22nm process technologies.

Tessera is suing **Sony** and **Renesas** claiming lapsed licensing of its packaging technology, and logged a complaint in US District Court against **UTAC** for breach of contract.

Four new members have joined the eBeam Initiative: **Abeam Technologies**, **EQUIcon Software**, **Synopsys**, and **TOOL Corp.**

NORTH AMERICA

With great sadness yet fondness we say goodbye to Selma Uslaner, one of *SST*'s first editors back to our inception in 1958, who passed away in late September. Her contributions to *SST*, the industry—and a generation of women in electronics—are legendary.

ATREG has spun out of real estate firm Colliers to offer transaction advisory services for "cleanroom technology manufacturing" in semiconductors, solar, and data centers.

Edwards Vacuum has broken ground at its new $1.5M, 55,000+ ft^2 headquarters in upstate NY.

ISMI is offering a Web-based calculator to track equipment performance (e.g. MTBF, MTTR, MTOL) for SEMI E10-conformant reporting.

Honeywell Electronic Materials is expanding production capacity for 300mm sputtering targets and raw materials.

Danaher is acquiring **Keithley Instruments** in a cash deal valued at ~$300M.

Cree has opened a new 150mm LED wafer production facility in Research Triangle Park, NC.

ASIAFOCUS

Elpida Memory reportedly is considering investing in some Taiwanese DRAM makers, in order to close its gap with rival Samsung.

TSMC has received the Taiwan government's green light to upgrade its Shanghai fab to 0.13µm process technologies.

ChipMOS has settled a breach-of-contract dispute with **Spansion** for $68M, half the $135M it had sought.

STATS ChipPAC has opened a 300mm embedded wafer-level packaging BGA (eWLB) fab in Singapore.

A "major logic foundry in Asia" has placed a multisystem order for **Ultratech**'s LSA100A laser spike annealing tools for its 40nm ramp.

Researchers at S. Korea's **Sungkyunkwan U.** have developed a low-temperature (40°C vs. 120°C) method for making graphene.

EUROFOCUS

Andre Geim and Konstantin Novoselov of the **U. of Manchester** have won the 2010 Nobel Prize in Physics for their work in graphene.

CEA-Leti and **SPP Process Technology Systems** have agreed to develop and optimize etch and deposition technologies for high aspect ratio 300mm through-silicon via (TSV) 3D IC processes.

IQE is planning a share sale to raise £20.8M in order to fund its acquisition of Sb substrate supplier **Galaxy**, expand manufacturing capacity, and repay debt.

The European Commission has granted €21M in loans and grants to **Mapper Lithography** to fund its e-beam litho efforts. ■

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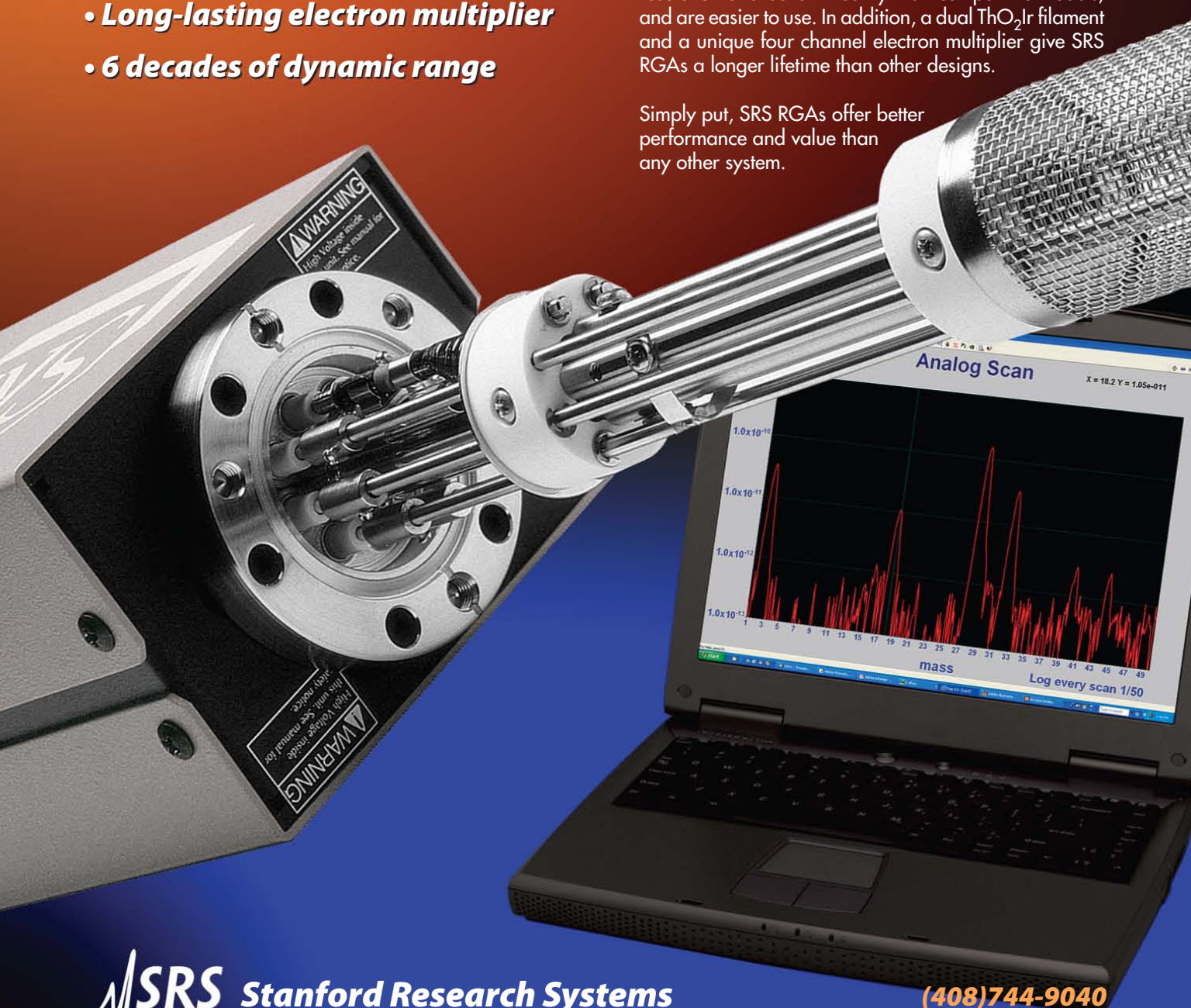

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TECHNOLOGY NEWS

Low-*k* dielectric family introduced by SBA Materials

Since Intel's Bohr published his seminal paper on interconnect scaling in 1995, the IC community has been searching for a manufacturable low-*k* dielectric which could scale to below *k*=2.0. The *ITRS* requirements for low-*k* have been continually relaxed due to the difficulty in achieving an electrically reliable, manufacturable process with either spin-on organic or inorganic dielectrics or C-doped CVD materials. Chemical and equipment companies, and the IDMs and foundries, have spent hundreds of millions of dollars trying to find this "holy grail." Technical articles over the last decade have documented issues such as CTE and fracture toughness that have arisen when trying to integrate highly porous low-*k* dielectrics.

The most recent *ITRS* roadmap (2009) indicates that low-*k* introduction to manufacturing has followed this timeline:

	90 nm	65 nm	45 nm
k =	3.0	30	2.7–2.8

Now, as dense carbon-doped oxides *k*=2.8) attempt to evolve into porous carbon-doped oxides with "ultralow" *k*<2.5 (ULK), there have been widely reported problems in manufacture, test, assembly, and packaging of these fragile chips. Most fabs and foundries have reported that they are struggling to see their way to a manufacturable *k*<2.5 solution. In fact the 2009 ITRS roadmap points to a "red brick wall" when attempting to go past k_{eff}=2.5.

	Units	uLK–120	uLK–122	uLK–124
Dielectric constant		2.0	2.2	2.4
Leakage	A/cm^2	10^{-11}	10^{-11}	10^{-11}
Breakdown voltage	MV/cm	>5	>5	>5
Modulus	GPa	6.0	7.3	8.6
Hardness	GPa	0.8	1.0	1.2
Fracture characteristic		Ductile	Ductile	Ductile

Several years ago, SBA Materials CTO Mark Philips and his team started developing "block polymer templated inorganic oxides" (US Patent #6,592,764) which self-assemble into materials with controlled structure and physical properties. These spin-on dielectrics (SBAM uLK) combine an amphiphilic block copolymer (structure-directing template) with silicon alkoxide esters. The block copolymer and silicate esters are self-assembled and the silicon compounds are polymerized to form mesoscopically structured silicon composites. The template is then removed (thermal, UV and/or e-beam) leaving a porous alkylated silicon dioxide low-*k* dielectric.

Properties of three grades of the new dielectrics are shown in the above table.

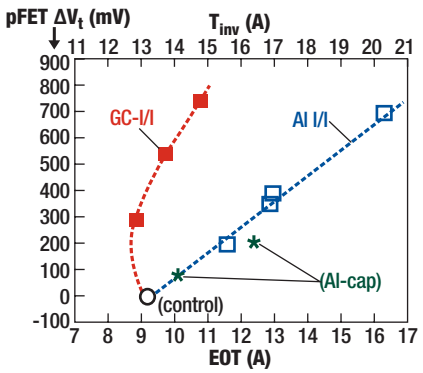
Microindent photos of uLK 124 show a clean ductile indent vs. many of the low-*k*

IEDM preview: IBM Alliance simplifies pFET HKMG process

Researchers from the IBM Alliance have developed a new germanium ion implantation process that implants Ge into the shallow silicon channel region prior to high-*k*/metal gate (HKMG) stack depositions. The process allows superior low threshold voltage (V_t) modulation relative to aluminum or titanium caps for low-V_t pFETs. At the 16nm node, such an approach could eliminate an aluminum cap and solve the low-V_t problem. Ion implantation also overcomes the integration challenges associated with epitaxial SiGe channel formation, which requires hardmask integration and precise silicon recess and SiGe thickness control. The group that developed the process, from Toshiba America Electronic Components, IBM's Semiconductor Research and Development Center, and STMicroelectronics will present their findings at the upcoming IEDM in San Francisco, CA (Dec. 6-8).

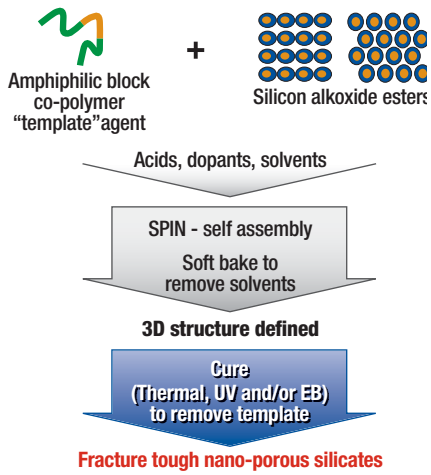
To achieve low-V_t modulation, the researchers compared Al to Ge channel ion implantation processes. The Ge implant was followed by a recrystallization anneal, interfacial layer formation, then HKMG deposition. undesirable hump in the C-V curve could be eliminated, the group determined, by using a cryogenic process in which wafer temperature was reduced during implantation. The Ge implant proved superior to the aluminum process because it lowered threshold voltage by as much as 500mV with no increase in equivalent oxide thickness (EOT, see figure). Conversely, large degradations of EOT occurred with the aluminum ion implantation. Other electrical results were favorable including an improved gate leakage current density/EOT curve (J_g-EOT), low gate-induced drain leakage (GIDL) current, and slightly improved NBTI characteristics over the control.

To better optimize the process, the researchers sought to determine the physical cause of the threshold voltage modulation. Backside SIMS revealed high Ge concentration near the gate stack/silicon interfaces, and the V_t shift correlates well with the



Threshold voltage shift vs. EOT. The germanium channel ion implantation induced ~500 mV threshold voltage shift with no increase in inversion thickness. The aluminum ion implant provides large V_t shift but also large EOT degradation. (Source: IBM Alliance)

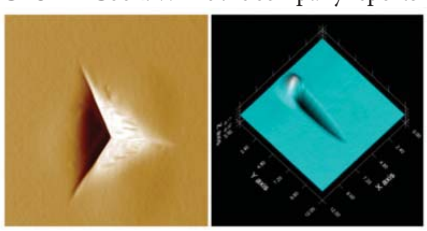
germanium peak concentration. Through a process of elimination and chemical analysis, they determined that pile-up of Ge atoms at the interfacial layer/channel interface determines the pFET threshold voltage shift. This physical cause of V_t modulation is completely different than that of a conventional epitaxial SiGe channel, where energy-band modulation is the key factor. — ***Laura Peters, contributing editor***



materials currently available which show brittle fracture during such testing.

The uLK materials can be integrated into existing fab lines using equipment and process flows already in place, according to the company. While spin-on materials would be a change for IC fabs that currently use CVD ILD dielectrics, CTO Phillips insists that this has not been a problem with current customers since spin coating is a well-known technique for materials deposition.

SBA has agreements in place with Asian chemical producers to manufacture, bottle, and supply under their label, to ensure quantity and IC grade quality that a start-up would not be trusted to deliver, reveals SBA CEO Bill Cook. While the company reports



that their uLK materials "...are in advanced qualification at three of the top 10 IC fabs in the world," they are not ready to reveal exactly who yet, because of secrecy agreements that are in place. It is thought that all three of the lead customers are in Asia.

The company is currently working with IMEC, and work on their first SBAM uLK processing paper was to be jointly presented at the Advanced Metallization Conference in Albany, NY in early October. — ***Dr. Philip Garrou, contributing editor***

IEDM: IM Flash details 25nm NAND

Also presenting at next month's IEDM, Intel and Micron researchers will reveal the key process advances and electrical results behind their multilevel cell (MLC) 64Gb NAND flash memory technology. At the start of 2010 their joint venture, IM Flash, said it was planning to ramp production of its 3bits/cell 64Gb NAND flash by year's end.

In this 25nm device, aggressive scaling in both the word line and bit line directions increases word line-word line capacitance as

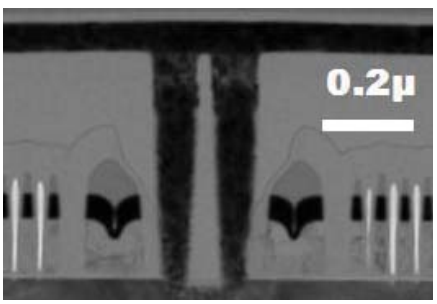


Figure 1. NAND cell in the word line direction shows the select gate and contacts. Air gaps reduce cell-cell and word line-word-line capacitance. (Source: Micron Technology/Intel)

well as cell-cell interference. Half pitches of only 24.5nm between word lines and 28.5nm between bit lines allowed a cell size of 0.0028µm^2. The researchers used air gaps (see figures) to reduce total interference by 25% and bit line capacitance by 30%. They also optimized the insulating tunnel oxide and inter-poly dielectric of the cell as well as surrounding dielectric to minimize leakage and charge trapping.

Another consequence of intense scaling is the effect on dopant fluctuation. The researchers note that at 25nm, threshold voltage can be expected to vary by ~30% due to random dopant fluctuation. This is countered by additional optimization of programming algorithms to achieve multilevel cell performance comparable to previous generations including its predecessor, the 34nm 32Gb technology.

The small die size of the 64Gb NAND flash allows packaging in a standard TSOP.

In January, IM Flash was reportedly leading the NAND flash technology-node race among contenders Samsung, Toshiba, Hynix, and others. Elpida (and Spansion) plans to start shipping samples of 1.8V 4Gb NAND flash memory during 4Q10, and will begin mass production during 1Q11.

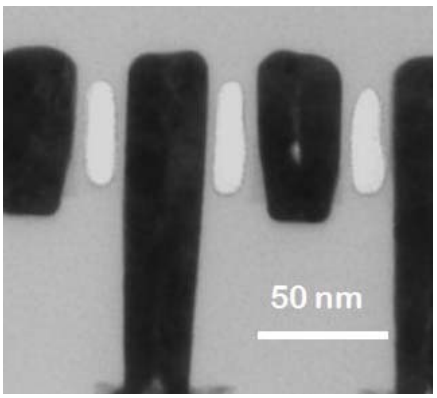


Figure 2. Bit line half pitch is only 28.5nm, requiring air gaps to reduce bit line-bit line capacitance. (Source: Micron Technology/Intel)

The industry is gradually making a transition from 2-bit multilevel cell to 3-bit technology (X3). Earlier this year, SanDisk's Eli Harari told *SST* that from 2010-2013, he sees the transition from MLC to X3 for about 50% of NAND bits. For SanDisk, X3 provides more than 20% more die per wafer compared to standard MLC memory on the same technology node. — ***Laura Peters, contributing editor***

 continued from page 11

BACUS: DFEB mask, EUV gets Brion boost

At the Annual SPIE/BACUS Symposium 2010 (Sept. 13-16), the eBeam Initiative had several members jointly presenting the latest achievements related to an design for e-beam (DFEB) manufacturing approach, showing the effectiveness of DFEB mask technology on advanced photomasks at the 22nm node and beyond.

A key demonstration at BACUS was the first demonstration of improved shot count results of writing curvilinear features using overlapping e-beam shots, Aki Fujimura, CEO of D2S and managing sponsor of the Initiative, told *SST*. "Due to the collaborative efforts of the eBeam Initiative members, we continue to make progress on the DFEB mask technology roadmap," he said.

For 22nm process technologies, the ability to use curvilinear features for mask lithography becomes critical. DFEB mask technology makes cost-effective, optical lithography for 22nm a reality by leveraging the rounding nature of e-beams to enable practical turnaround times for complex and curvilinear features. The collaborative results from the eBeam Initiative members further demonstrate the ability of DFEB mask technology to enable fewer shot counts and less write-time than traditional e-beam writing techniques on advanced photomasks.

Also at BACUS, Brion Technologies debuted its Tachyon NXE software to optimize predictive modeling for parent company ASML's extreme ultraviolet (EUV) scanners, claiming it can reduce development time and cost to produce chips on the EUV systems.

The Tachyon NXE software package integrates with existing Tachyon products to enable EUV lithography process simulation. To develop the EUVL simulation models, TwinScan NXE:3100 scanner characteristics were incorporated to model the optical performance. By simulating the behavior of the new scanner, Tachyon NXE can efficiently predict and correct NXE-specific effects before the start of chip production, helping to decrease EUV mask re-spins and shorten the learning cycles during final mask development.

Brion's applications for optical proximity correction (Tachyon OPC+) and lithography manufacturability check (Tachyon LMC) can now incorporate the new software model of ASML's EUV pre-production scanners, six of which are slated to ship before mid-2011, and have been optimized for EUV requirements of accuracy, file size and run-time. In multiple DRAM test cases, the company says it has demonstrated the capability to perform full-field (~8cm^2)

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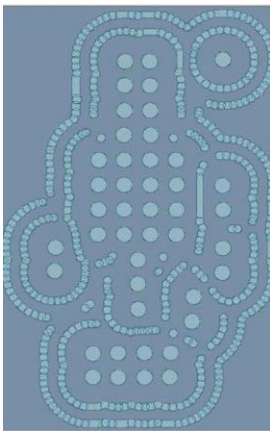
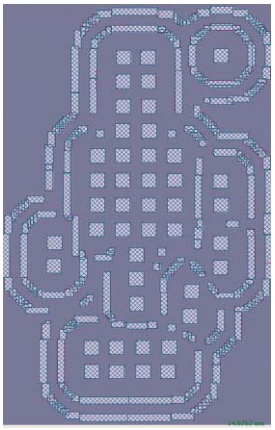
Ideal mask



484 circle + VSB shots
Better CDU with circular main features

D2S optimized DFEB mask



402 overlapped VSB shots (unassigned dose)
vs. ~620 conventional shots

Left: Circular and variable shaped beam (VSB) shots used to shoot an inverse lithography technology (ILT) mask for a contact layer at the 22nm logic node incorporating circular and curvilinear features using design for e-beam (DFEB) mask technology. Right: VSB shots used to shoot a Manhattanized ILT mask with rectangular main features using DFEB mask technology. This mask would produce nearly identical wafer lithography quality as the mask printing at left. Using D2S' Model-Based Mask Data Preparation (MB-MDP) engine, this pattern is produced with 402 overlapping VSB shots versus 620 VSB shots with conventional fracturing. Only rectangular VSB shots are used.

Trends and technologies for CMP in hard-disk drives

About 40 fellow techno-geeks attended a Sept. 15 meeting of the NCCAVS CMP Users Group at SEMI headquarters in San Jose, CA, with an agenda comprising seven topics for a combination of technical, technical marketing, and marketing presentations, all with the theme of chemical mechanical planarization (CMP) for the hard-disk drive (HDD) industry. The group will post proceedings and presentations in the coming weeks.

Opening the meeting with a HDD market overview was John Kim of Trend Focus. Growth in the HDD sector has dropped from 15% CAGR in 1998-2007 to 10% for 2008-2014, with seasonal stability provided by strong markets in the BRIC region (Brazil, Russia, India, China), he said. By 2014, the majority of drives will be in the 1Tb-2Tb range. At the same time, solid-state drives (SSD) will comprise 5%-6% of the market, even though the upper size will still be in the range of 128Gb. The consumer appetite for larger and larger drives has shown no evidence yet of an upper limit.

Western Digital's Sungpyo Jung talked about consumables challenges in magnetic head CMP. Production uses 150mm AlTiC substrates, a wafer size not actively supported by all equipment manufacturers. Slurries use alumina abrasive with different chemistries to planarize features of Al_2O_3, magnetics (NiFe, CoNoFe, CoFe), metals (Au, Cu, CoPt, Ta, Ti, Cr, Ru, etc.), and photoresist. Performance metrics are familiar to semiconductor CMP engineers, but their rank importance is different for HDD. Within-wafer uniformity improvement is a key unmet need.

Kristan Bhatten of Dionex introduced a new-generation ion chromatography tool with a 0.4mm capillary and 0.4µL sample injection volume. The tool is expected to be useful for characterizing substrate surface contamination down to ppt levels, but specific data sets to showcase the tool for HDD and semiconductor CMP are still being developed.

Haijing Peng of KLA-Tencor showed a non-contact eddy current alternative to a four-point probe for measuring sheet resistance and polishing rates. The non-contact characteristic makes it possible to monitor processes on product wafer, eliminating the expense and throughput overhead of monitor wafers.

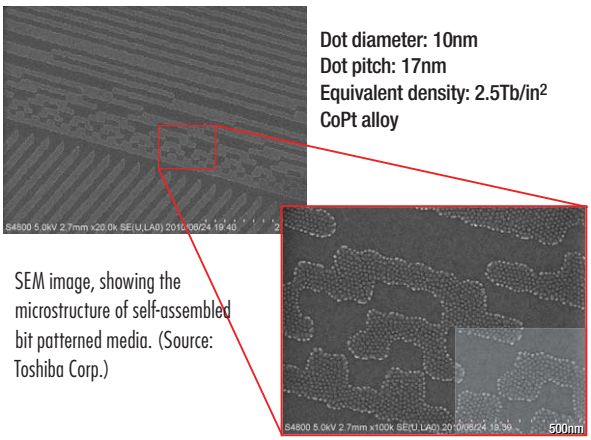
continued on page 31

Diskcon: Toshiba's bit patterning, Samsung's HDDs

At DISKCON 2010 (Sept. 9-10, Santa Clara, CA), Toshiba Corp. presented details behind its use of bit-patterned media (BPM) to fabricate a hard disk with an areal density of 2.5TB/in^2 and a practical servo pattern. According to the company, BPM technology is a leading candidate to achieve terabit-class high density HDD recording, which could result in 25TB of data on one 3.5" drive. The company anticipates practical application of BPM technology around 2013.

The microstructure of the self-assembled bit-patterned media (BPM) is visible in the figure below. An etching mask enabled Toshiba to lay down the dots in a servo pattern, shown in the enlarged area, readable by a hard drive. Each dot—a single magnetic grain 17nm in size—is one bit.

Also at Diskcon, Samsung Electronics responded to consumer demand for high-definition content with new products in optical disk drive (ODD) technology, and rapid growth from 2-3TB to 4TB HDDs in 2011. Richard Aguilera, national sales manager at Samsung Electronics, outlined the company's optical disk drive division product roadmap and summarized the market drivers, especially high-definition (HD) content, highlighting new products particularly in the BluRay sector. In the second half of this year, the company will come out with a 12X writer that will enable the consumer to write HD content and record it to an optical disk drive (ODD) and play it back on a consumer device. The company is also addressing the legacy market with new SATA and PATA formats.



SEM image, showing the microstructure of self-assembled bit patterned media. (Source: Toshiba Corp.)

Albert Kim, director of sales for storage products at Samsung Electronics, noted how the consumers' drive to store/save content, (videos, photos, music, etc.) is driving mass storage devices. After releasing a 2TB (3.5in. desktop drive) HDD at DISKCON 2010, the company will be releasing a 3TB drive, and then a 4TB drive in 2011. — ***D.V., J.M., M.C.***

Check out Debra Vogler's interviews with Toshiba and Samsung execs at www.electroiq.com/podcasts.html.

CMP for metal-gate integration in advanced CMOS transistors

EXECUTIVE OVERVIEW New materials complicate the process integration in high-volume manufacturing of high-*k* metal-gate (HKMG) CMOS transistors. The gate-last HKMG process requires two new CMP processes, both requiring extreme control over final gate height and topography. Because the gate stack is at the heart of the active device, it is far more sensitive to dimensions compared to passive interconnect and isolation structures. The poly-open CMP process has been tuned to handle new selectivity challenges. A new family of aluminum CMP slurries has been developed to provide <10nm dishing regardless of the layout. The methodical tuning of slurry additives provides for the successful integration of both poly-open and Al CMP into HKMG process flows.

For over twenty years of IC manufacturing, the creation of planar device structures has required the use of technologies to reduce topographic variation. Chemical-mechanical planarization (CMP)—pressing wafers into rotating pads in the presence of special slurry blends to produce removal through chemically amplified nano-scale abrasion— has become a critical part of modern IC fabrication.

The initial application of CMP technology was to planarize silica dielectrics for interconnects. This early use of CMP was driven by the need for basic planarity. It reduced the depth-of-focus requirement for the microlithography used to pattern the dielectric and metal layers. However, in part due to the empirical nature of original CMP process development, the technology had historically suffered from poor process control. A technology ecosystem of users, OEM's, specialty materials suppliers, and academics recognized the challenge and worked together to ensure that CMP can meet the evolving needs of the state-of-the-art in IC fabrication. This led to the adoption of CMP for a wider variety of uses.

The first metal CMP application in manufacturing was for tungsten (W) plug formation prior to the 0.35µm node. CMP processes for polysilicon (poly), shallow trench isolation (STI), and copper (Cu) were developed and deployed to solve problems in the quest for continued scaling. Also, as the requirements for CMP have become more difficult, it is now typical for the overall material removal in a CMP process to be broken into multiple specialized steps, often with unique consumables.

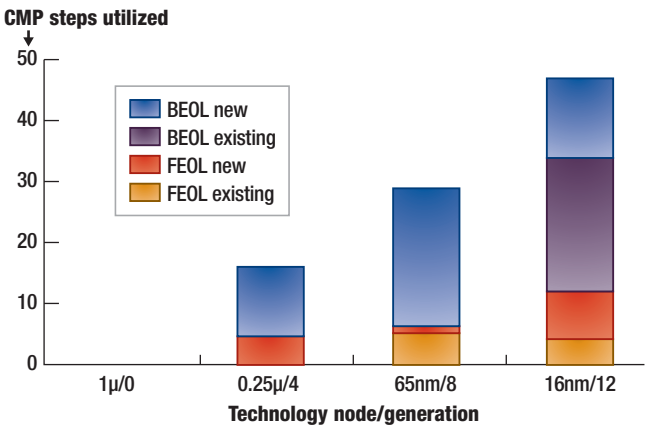


Figure 1. Starting from the 0.25µm node, about four new CMP steps have been added with each new CMOS technology generation.

Scaling and planarization of materials

CMOS scaling has led to transistor devices with critical structures approaching a few atoms in size. New materials and new structures of existing materials have been found to optimize device size and performance.

Many of these changes in IC device structures and materials have driven new planarization requirements. **Figure 1** shows that since the era of 1 micron minimum features, a net average of four CMP steps have been, or are being added, with each new CMOS manufacturing technology node [1].

The replacement of traditional materials for the gate dielectric and gate conductor has recently been a major focus for our industry. Traditional CMOS transistors are made with silicon-oxide/nitride (SiON) gate dielectrics and polysilicon gate conductors. The dielectric begins to suffer worse leakage as the dielectric thickness gets into the single-digit range of atoms. More exotic dielectrics are needed to resist leakage while managing other fundamental device parameters.

High-*k* metal-gate (HKMG) transistors were first implemented with 45nm technology. The dielectrics are based on oxides of hafnium, which can maintain low electrical leakage levels. The polysilicon conductors also need to be replaced because they do not work well with the new dielectrics. The NMOS and PMOS transistors require independently optimized complex stacks of thin work-function metals topped by a bulk conductor layer.

There are different flows under development for 32nm node processing, depending upon whether the metal-gate is formed before or after the source and drain regions. The source and drain

Paul Feeney, CMP Fellow, Cabot Microelectronics Corp., Aurora, Illinois, USA

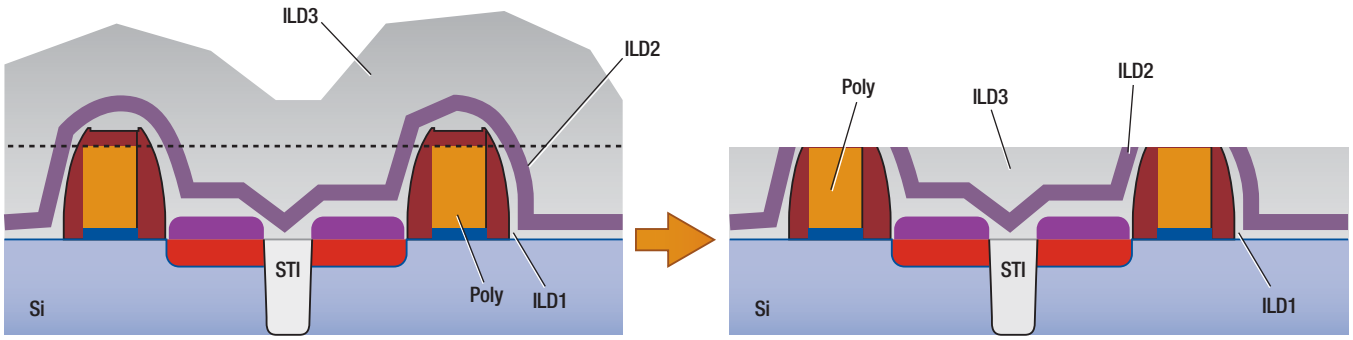


Figure 2. Cross-sectional schematics of "gate-last" CMOS transistors before (left) and after (right) the "poly-open planarization" (POP) CMP process, showing that this step controls the height of the sacrificial-poly gate.

formation includes high-temperature steps such as implants and anneals, so forming the gate first restricts the choices of conductors that can be successfully integrated. In contrast, forming the gate last—also known as the replacement metal gate (RMG) process flow—allows for the use of aluminum (Al) as the bulk conductor and has gained momentum. There is also the possibility of a hybrid approach where NMOS transistors are formed gate-first while PMOS transistors are formed gate-last.

As the device structures have become more complex, so have the manufacturing processes needed to form them. The gate-last (RMG) HKMG process flow is initially almost identical to that used to form traditional SiON/poly gates. Only after all of the high-temperature process steps are complete are the poly gates etched out and replaced by metal. The essential flow is as follows [2]:

1. STI, implants for wells and V_T control,
2. ALD of high-*k* gate dielectric and poly deposition,
3. Lithography and gate etch,
4. S/D extensions, spacer, Si recess and SiGe deposition,
5. S/D formation, Ni salicidation, ILD_0 deposition,
6. Poly open CMP, poly etch,
7. PMOS work-function metal deposition,
8. Metal gate lithography and etch,
9. NMOS work-function metal deposition, and
10. Al metal gate fill and CMP.

CMP for gate-last HKMG

Since the gate is essentially at the heart of the transistor, extreme control is needed over all gate processing steps to ensure proper device function. Control is made even more challenging by the atomic-scale dimensions in advanced devices. Variation in gate height of just a few atomic layers now leads to measurable transistor performance variability [3].

CMP is central to the above integrated gate-last process flow, being used in two challenging processes to form the active device. The new dielectric process—referred to as poly open planarization (POP) CMP —has several additional challenges compared to the oxide polish utilized for making standard devices. **Figure 2** shows that the transistor structure includes a combination of oxide, nitride and polysilicon films instead of just oxide.

A preferred way to address the total removal is to first polish the oxide back to the nitride in a step that is very similar to what is done in STI CMP today. Then, a final step is used to expose the tops of the polysilicon features. The process in this final step must remove the correct amount of each film while preventing local topography from being generated due to the film differences. Compared to a traditional ILD0 CMP step, even tighter thickness control is required in order to manage the height, and thus resistivity, of the gate conductor.

After the STI-like step, the nitride will be raised versus the oxide, so it is desirable for planarization to have the nitride removal rate above the oxide rate. Typical Silica-based slurries for the planarization of oxides have nitride to oxide selectivity well below 1 and have material removal rates too high for easy control.

New ways were found to produce a moderate nitride removal rate. The nitride removal mechanism is dependent on hydrolysis of the Si_3N_4 to Si-OH and NH_3 [4]. This reaction is pH dependent, with low pH being faster. At very low pH, silica is less anionic and is not as attracted to the nitride surface, which leads to a lower removal rate.

A new slurry platform, iDiel N3100, was produced. The silica particles in this slurry are uniquely charged to boost attraction to the to the dielectric. In this system, the oxide removal rate is controlled by pH (**Fig.3**). The oxide removal rate is affected by the presence of the nitride, so the removal rate on patterned wafers starts higher

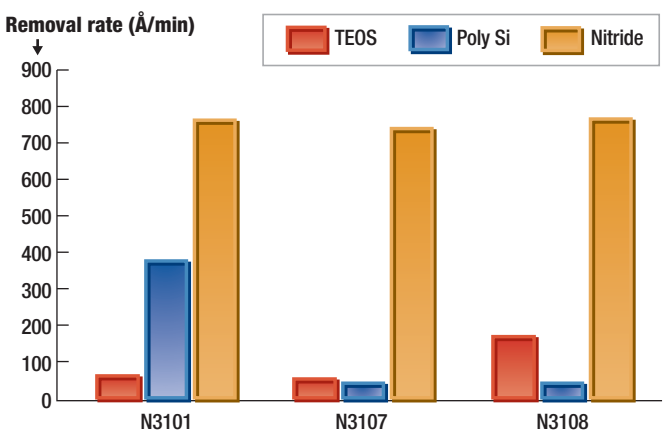


Figure 3. A range of blanket removal rates are possible through the use of additives to suppress poly removal and pH to accelerate oxide removal in the iDiel N3100 slurry family.

CMP continued from page 15

and then slows as the nitride being removed decreases. This results in the prevention of local step heights. The polysilicon removal rate is driven down by additives (**Fig.3**). Having a low polysilicon rate and a slowing oxide rate improves the ability of the process to stop at the desired thickness target.

RMG Al CMP

The new metal CMP process—referred to as the replacement metal gate (RMG) aluminum CMP step for this gate-last flow—also has significant challenges compared to that used for W contacts. The process must planarize Al and the complex stack of work-function metals. It also must do so while stopping well on oxide and minimizing recess, both of which contribute to the gate conductor final height.

The advent of replacement metal gate (RMG or gate-last) HKMG process flows for 45nm node and below CMOS manufacturing has led to a significant amount of development going into the new dielectric and metal CMP steps. The needs are now being met with processes using consumables designed specifically for these steps.

The Novus A7100 series of slurries was designed with alumina particles that provide the ability to remove Al and the work-function metals selective to the oxide underneath. As in the polishing of other metals, oxidizers and chelators play a role in creating passivation and ion-complex formation, but the mechanisms employed are unique in this system.

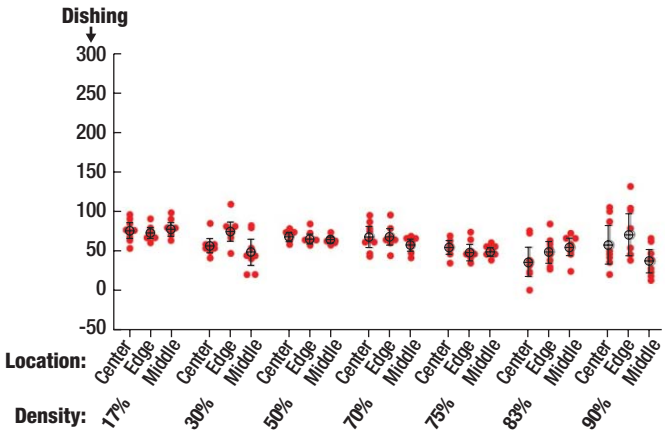


Figure 4. Within-die non-uniformity (WIDNU) data from Al CMP using A7100 slurry on a D100 pad, showing good control across a wide range of feature densities (95% CI for the mean).

There are significant ways in which Al CMP is different than other metals. In W CMP, oxides of W are formed that are softer than the bulk metal and are removed more easily. Oxidation of Al creates a surface that is harder than the bulk film. This aluminum oxide surface is critical in slowing removal after clearing the bulk film in order to minimize recess. CMP using the series slurry noted above roughly follows Preston's Law—removal rate is a linear result of pressure and velocity—demonstrating the mechanically limited nature of removal.

This passivation and removal mechanism leads to other differences. In CMP of Cu, a technique called a soft landing—where pressure is decreased during clearing to slow removal—is a common approach for minimizing recess at the expense of process time. In the Al system, higher pressure actually improves recess.

Too much mechanical energy has, however, a unique downside here. As the nano-abrasion from the particles increases, it can overcome the kinetics of passivation. The result is abrasion of the soft bulk Al that leads to a buildup of "black debris" on the polishing pad [4]. This debris is comprised of small Al particles that remain dark in color for a short amount of time until they become fully oxidized. At the onset of black debris, removal rate and defectivity both change significantly.

The optimal Al CMP process balances rate and recess (**Fig.4**) versus debris and defects. Recess levels are below 10nm across a wide range of feature sizes and densities after the aluminum CMP step. This recess can be further reduced by an optional buff step that removes a very controlled amount of dielectric.

Conclusion

As CMP technology has matured, it has become a more attractive option for wafer processing. In addition, CMOS device scaling has led to a steady increase in the number of CMP steps, due to both an increase in the number of layers, as well as a need to create novel structures with exotic materials.

The advent of replacement metal gate (RMG or gate-last) HKMG process flows for 45nm node and below CMOS manufacturing has led to a significant amount of development going into the new dielectric and metal CMP steps. The needs are now being met with processes using consumables designed specifically for these steps.

Acknowledgments

Many thanks to scores of people across Cabot Microelectronics and our industry for their contributions to these technologies. Novus, iDiel, and Epic are trademarks of Cabot Microelectronics Corp. ■

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Biography

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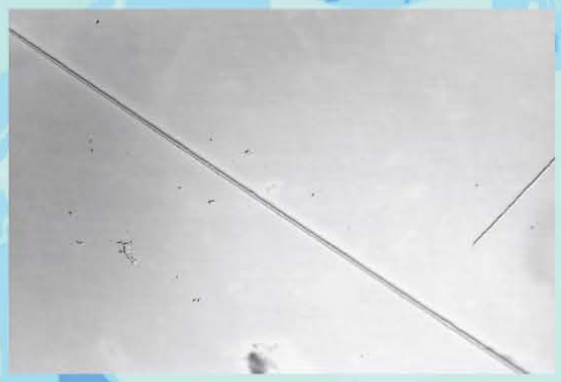
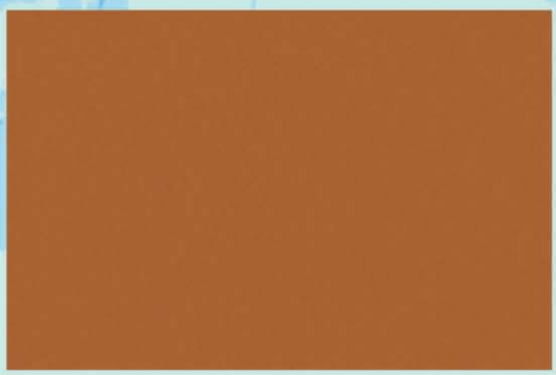


ULK wafer polished with slurry which was recirculated 1000x with a bellows pump

AFM image of wafer surface polished with slurry which was recirculated 1000x with a bellows pump

With Levitronix Pump

ULK wafer polished with slurry which was recirculated 1000x with a Levitronix pump



AFM image of wafer surface polished with slurry which was recirculated 1000x with a Levitronix pump

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ATOMIC LAYER DEPOSITION

Atomic layer deposition goes mainstream in 22nm logic technologies

EXECUTIVE OVERVIEW Atomic layer deposition (ALD) will be used in multiple areas of the 22nm logic process flow despite initial concerns about the technology's viability for high-volume manufacturing. Each application space creates a unique need for manufacturing equipment configuration and technology variations – from single-wafer ALD systems for extremely tight process control, batch ALD systems for low COO operation, to mini-batch systems for a meld of COO and process control for multi-layer applications. Selection of the appropriate manufacturing toolset is as critical to eventual technology adoption as the process itself, and final implementation will require the correct toolsets to ensure that the ALD films can be deposited in a cost efficient manner.

Since its invention in the 1970s, atomic layer deposition (ALD) has been used in a variety of applications ranging from electroluminescence display manufacturing to industrial coatings [1]. Over the last decade, the semiconductor industry has slowly been adopting ALD reactors for critical layers where the benefits of ALD enable scaling and improved performance. With the upcoming transition to 22nm, process flows are being adapted to allow ever more ALD layers. As a variant of chemical vapor deposition (CVD), ALD techniques capitalize on surface saturation reactions to deposit extremely smooth, dense, and highly conformal films through a process that is relatively insensitive to fluctuations in process temperature and reactant flux. The ALD process relies on sequential introduction of the reactants into the reaction space, separated by inert gas purges, such that repetition of the ALD cycles results in a monolayer by monolayer growth of the deposited film. Thickness of the film can then be precisely controlled by adjusting the number of ALD cycles.

Process considerations for single-wafer tools

DRAM manufacturers were the first to use ALD to ensure conformal deposition of high-*k* dielectrics in high aspect ratio capacitor structures. Aggressive scaling of device dimensions and the subsequent requirement of low thermal budgets to control dopant diffusion continue to push the entire semiconductor industry to displace conventional CVD, plasma enhanced CVD (PECVD), and sputtering techniques with novel ALD processes in critical areas such as transistor gate stack formation and spacer defined double patterning. The low throughputs that are typically associated with ALD techniques have been a barrier to its adoption in mainstream production flows. However, these concerns are being addressed by intelligent equipment design to optimize the ALD process and hardware for individual application spaces. At the 22nm node, the logic industry will use ALD in several key process steps – both in front end transistor formation and in back end metallization and interconnect. Each application has highly specific requirements and calls for different hardware configurations for the optimal production solution.

Single-wafer ALD chambers are ideal when the application demands extremely thin films with precise thickness and uniformity control. Single-wafer systems can also most easily handle difficult precursor chemistries such as low vapor pressure, decomposition prone liquids and solids since ALD cycle times are typically short (in the order of a few seconds) and the source delivery systems can be placed in close proximity to the reaction chamber. Purge efficiency can be optimized relatively easily in single-wafer systems and as a result, these chambers are ideal for pure ALD deposition.

Single-wafer ALD systems also have high precursor utilization efficiencies and hence, are a good fit for processes that use expensive precursor materials. For example, high-*k* dielectrics and metal gates for transistor gate oxide and electrodes require deposition of films as thin as 10Å while maintaining within wafer uniformities of <1%, 1σ. Hafnium-based high-*k* gate oxides typically use hafnium chloride, a solid precursor, for its excellent electrical performance when compared to metal organic chemistries [2]. Single-wafer systems tend to be the best choice for gate oxide deposition as they are very capable of delivering this highly condensable precursor. Furthermore, replacement gate devices require multiple, conformal metal films <50Å thick to ensure that space remains for a gate contact fill (**Fig. 1**). Single-wafer plasma-enhanced ALD (PEALD) is also used for the deposition of silicon oxide, silicon nitride, and silicon carbon nitride gate spacers. PEALD enables low-temperature deposition (<400°C), excellent conformality, and lower wet etch rates than films deposited by plasma enhanced CVD (PECVD). Film stress can also be varied from compressive to tensile by varying plasma processing conditions [3]. Techniques such as PVD and CVD are unable to attain the step coverage, thickness control, and cross-wafer uniformities required for such an application; single-wafer ALD has been gradually replacing these techniques in high performance logic gate structures since the

M. Verghese, ASM, Phoenix, AZ USA; **J. W. Maes**, ASM, Leuven, Belgium; **N. Kobayashi**, ASM, Tokyo, Japan

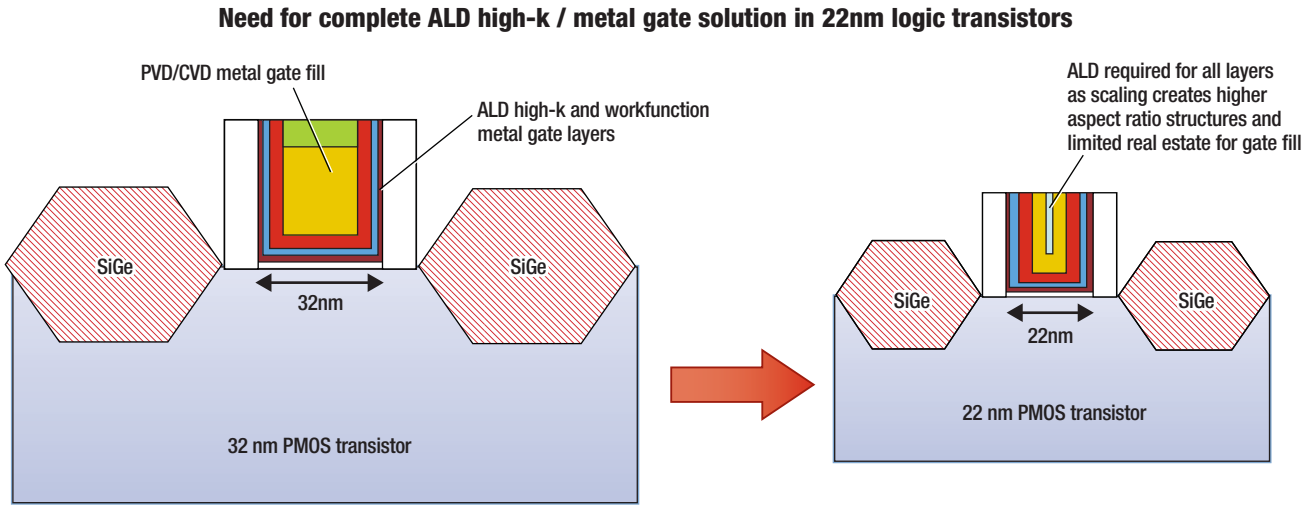

Figure 1. Need for complete ALD high-*k*/metal gate solution in 22nm logic transistors.

45nm node [4]. By the 22nm node, all primary gate stack materials will be deposited by ALD processes. The advent of three-dimensional architectures such as FinFETs, and the film conformality requirements that come therewith, will ensure that ALD will be the deposition technique of choice for the next several generations of advanced logic gate stack structures.

Batch tools for thicker films/high-aspect ratios

When film thicknesses are less than one hundred angstroms thick, ALD process times are typically no longer than a few minutes. Single-wafer tools then give acceptable throughput performance and short turn-around times. However, for some applications, the process times are inevitably longer. This can occur when thicker layers are required or when films have to be deposited in high-aspect ratio structures. Substrates with high-aspect ratio structures have a larger surface area than planar wafers and usually require a higher precursor dose and subsequently need longer pulses and purge times to enable effective gas transport into and out of the structures. Also, some ALD chemistries can have lower growth rates than others and some processes may require relatively long pulses to ensure complete surface reactions to achieve the desired film quality.

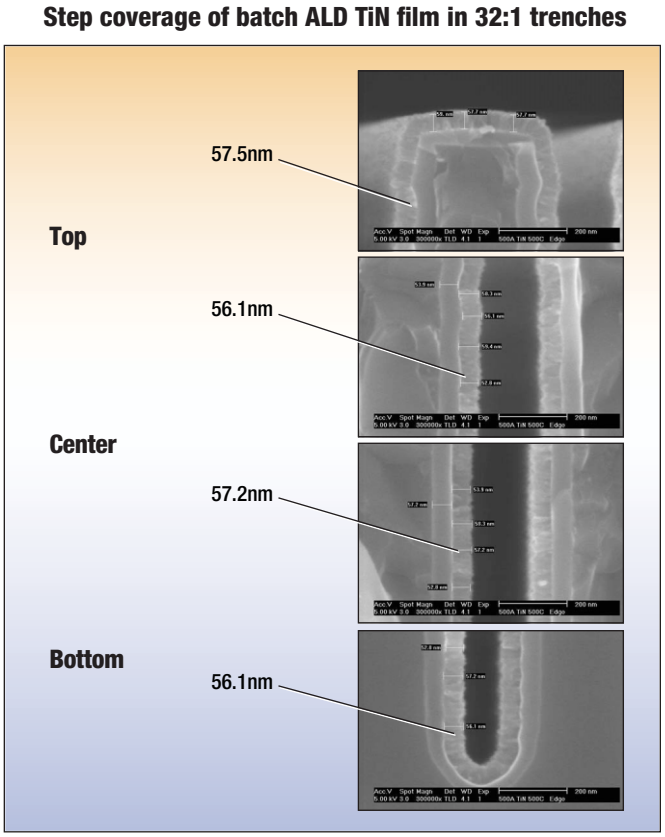

Figure 2. Step coverage of batch pulsed CVD TiN film in 32:1 trenches.

The throughput and cost-of-ownership (COO) performance of batch ALD approaches with ~100 wafer loads in one reactor can be substantially better than that of single-wafer systems. Pulse and purge times have to be longer in batch reactors because the volume of the reactor is larger and the gas transport depends more on diffusion (rather than forced convection) than in single-wafer systems. However, the total increase in cycle time is smaller than a factor of 100, more on the order of 10-50. Process optimization in a batch system is more complex than in a single-wafer system but for ALD chemistries that result in self-limiting ALD surface reactions, relatively good uniformities and step coverage can still be achieved. The precursor flow and total dose that is delivered to the batch reactor is typically much larger than in single-wafer applications, especially when high aspect ratio device structures are involved. However, techniques such as direct liquid injection (DLI) can be used to mitigate precursor dose delivery issues as long as the vapor pressure of the precursor is sufficiently high. Low vapor pressure precursors (which also can be solid powders) are more troublesome in batch equipment due to risk of condensation and decomposition associated with the high residence time in the reactors.

ALD titanium nitride using titanium chloride and ammonia meet all the criteria required to make batch processing an attractive option. Titanium nitride films are used in several applications in logic devices: electrodes for replacement gates, electrodes for embedded DRAM devices, barrier films in tungsten contacts, and through-

Atomic layer deposition continued from page 19

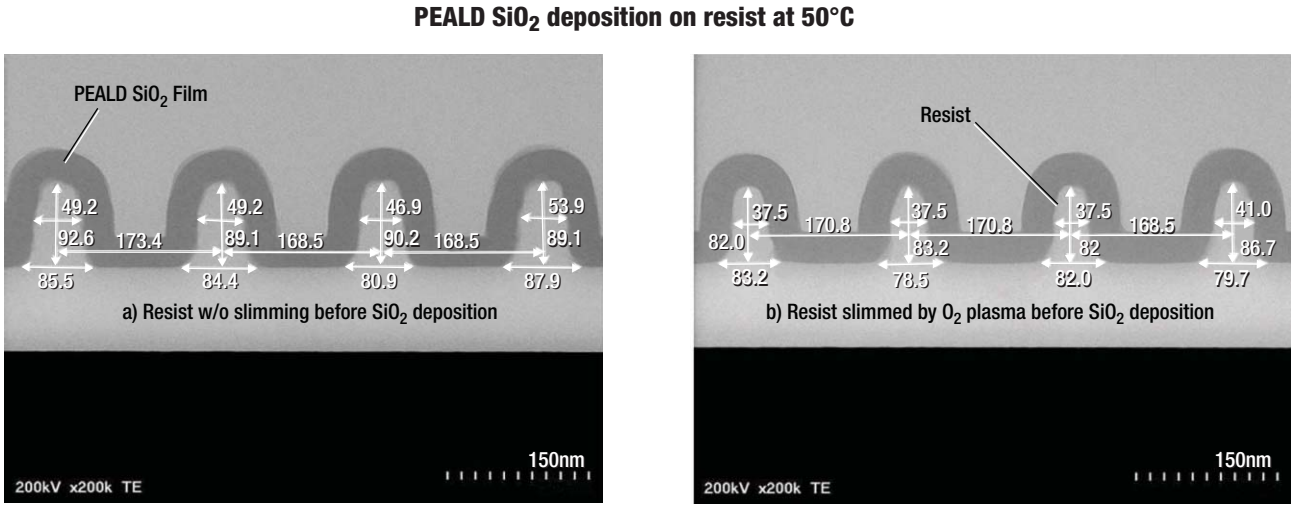

Figure 3. PEALD SiO_2 deposition on resist at 50°C.

silicon-via (TSV) structures. Required film thicknesses are in the range of 20–150Å.

The process can be run in two modes: a strict ALD mode where completely separated titanium chloride and ammonia pulses are used (resulting in a growth rate of ~0.3Å/cycle), but also in a second mode in which one of the two pulses is actually a CVD pulse. In the pulsed CVD mode, a higher (3-5x) growth rate can be achieved. Batch reactors are able to run ALD-like processes such as pulsed CVD, with good results. The resulting film resistivity is a function of deposition temperature. In the ALD mode, one can use about 100°C lower deposition temperature to achieve the same resistivity as films deposited by the pulsed CVD mode [5]. **Figure 2** shows an example of the deposition of a thicker layer of titanium nitride in a high aspect ratio structure. A highly conformal film is achieved, with step coverage of better than 95%, using the ALD-like pulsed CVD process mode in a batch reactor. Batch reactors can run at a throughput of greater than 30wph per reactor for 10nm films. These results demonstrate that batch-type ALD reactors are an attractive tool choice for some of the new ALD applications in future logic devices.

Mini-batch or multi-wafer ALD systems

When deposition of thicker films using complex precursors is required at reasonable throughputs and with short turn around times, a mini-batch or multi-single-wafer ALD system is the most appropriate. Mini-batch and multi-single-wafer ALD reactors meld the flexibility of single-wafer systems with the productivity of batch reactors. Typically, a mini-batch reactor processes four to five wafers together in one reactor and a multi-single-wafer system processes four to five wafers in individual reactors packaged in one module. These types of reactors can result in improved COO when compared to single-wafer systems as they occupy less floor space and rely on fewer, shared sub-systems. For example, gas panels, RF systems, and pumps can be combined for use on a mini-batch system whereas single-wafer tools would require multiple individual sub-systems. In addition, creative design of mini-batch systems can allow the use of direct plasma to enable plasma-enhanced ALD processes.

Spacer-defined double-patterning (SDDP) will likely be introduced to manufacture highly scaled lines and spacers for 22nm logic devices. In this technology, a conformal, ALD silicon oxide (SiO_2) film is deposited directly on photoresist at extremely low temperatures. This is followed by an anisotropic etch-back process that results in the formation of SiO_2 spacers that act as hard masks with smaller pitches. For this application, a mini-batch (multi-single-wafer) system is useful - ensuring high throughput in a system that can utilize direct plasma to enable deposition at near room temperatures. PEALD SiO_2 using a mini-batch system results in conformal deposition at low-temperatures (<100°C) with within-wafer and wafer-to-wafer uniformity < 1%, three sigma. Throughputs can be achieved at >45wph per reactor at 20nm film thickness with high equipment utilization due to in situ remote plasma cleaning capability.

One cycle of PEALD SiO_2 consists of 3 steps: chemisorption of an aminosilane precursor on the substrate, purging the precursor by inert gas flow, and plasma-assisted surface reaction of chemisorbed precursor with reactant gas. The RF-based plasma pulse is <400ms in length. Growth per cycle (GPC) of PEALD SiO_2 increases with decreasing deposition temperature [6]. This GPC temperature dependence indicates the ALD reaction is limited by the desorption rate of the physisorbed precursor, which increases with increasing deposition temperature. Because this is an ALD process, film thickness is proportional to cycle number and thickness can be precisely controlled. These PEALD films have been confirmed to not cause plasma damage to the underlying substrate/films as the RF power during the deposition process is much smaller (<50W) than that of conventional PECVD.

As shown in **Fig. 3a**, 300Å of a conformal SiO_2 film can be deposited directly on resist at 50°C without any damage. Furthermore, in situ treatments can be used to widen the space between lines and/or reform the resist shape. **Figure 3b** shows an example of in situ treatment before SiO_2 deposition. In this case, the resist is slimmed isotropically by ~65Å. Within wafer uniformity of the treatment process is typically <2%, 3σ. This is a good example showing the process flexibility gained by using

a mini-batch system, while sustaining the high throughputs required for manufacturing.

Conclusion

Overcoming the initial barriers to adoption has required the creation of several toolset configurations to address the unique issues in specific applications. Single-wafer, batch and mini-batch ALD solutions are available, each with thermal and plasma enhanced capabilities, and selection of the appropriate manufacturing toolset is as critical to eventual technology adoption as the process itself. In very cost sensitive markets such as memories, cost-of-ownership (COO) will be a main driver for equipment selection. In foundry or other logic applications, equipment choice is more a mix between COO, turn-around time and process performance considerations and choices of equipment type have to be made with careful regard to the specific application. ■

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Biographies

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REDISTRIBUTION AND FAN OUT

Dielectric materials evolve to meet the challenges of wafer-level packaging

EXECUTIVE OVERVIEW The role of dielectric materials in wafer-level packaging has evolved to meet the changing requirements of new and more advanced chip designs and packaging technologies. These advances in dielectric materials have paralleled changes to both the integrated circuits and their corresponding packaging methods. As consumers demand more functionality in smaller and lighter devices, more and more sophisticated ICs are being designed. This in turn has challenged packaging houses to come up with methods to connect these higher density ICs with their devices. New packaging methods are leading dielectric materials suppliers to adjust their chemistries to provide innovative products.

Polyimide dielectric materials have traditionally served as stress-buffer passivation layers (SBPs) on ICs that were wire-bonded to lead frames and encased in mold compound [1]. Two failure modes of this packaging scheme were stress-induced die cracking and molding compound delamination. Die cracking results from the stresses induced by the mold compound due to the mismatch between the coefficient of thermal expansion (CTE) of the molding compound and the silicon chip. If the mold compound delaminates from the surface of the IC, a void is created where moisture can permeate, leading to corrosion.

To alleviate these issues, a polymeric, secondary passivation layer is applied over the primary silicon nitride passivation layer. This secondary layer cushions the device from the molding compound stresses and provides better adhesion. Polyimide-based materials have historically been used for SBP layers due to relatively low stress levels, proven chemical resistance, and good thermal and mechanical stability.

Redistribution layers in wafer-level packaging

As the evolution of portable electronic devices progressed, all the components in the device had to become smaller, lighter, and higher-performing. Flip-chip packaging moved contacts from the bulky molded lead frame to solder balls on the surface of the chip. The IC was then simply flipped over and reflow soldered to the substrate in a much more compact manner [2].

To accomplish this, the wire bond pads located at the edges of the chip had to be re-routed or redistributed across the surface of the chip. There are several methods for this, but most involve adding a dielectric layer to the surface of the IC, selectively removing portions of the film to expose the original bond pads. On top of this dielectric layer are plated copper traces from the bond pads to the sites of the solder balls (**Fig. 1**). Often a second dielectric layer is put on to cover the copper traces. Solder is either screen-printed or placed and reflowed to form the solder ball grid on the top surface of the chip [3].

Polyimide materials were quickly adopted in this new application. New polyimide chemistries evolved that retained their good chemical resistance, thermal and mechanical properties but, in addition, were copper compatible, adhered well and had broad processing latitude. The most widely used materials are solvent-developed, meaning an organic solvent is used to develop away the polymer in the areas it was not needed. With the focus on more environmental stewardship, many manufacturing operations were looking to reduce their use of organic solvents.

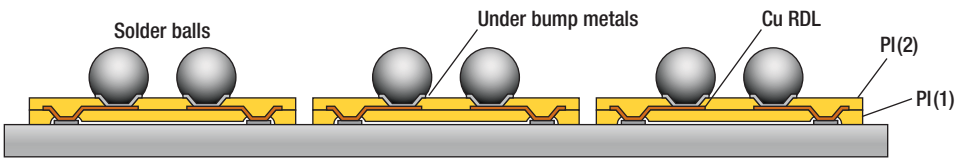

Figure 1. In redistribution layer packaging, the polyimide dielectric layers – shown as PI(1) and PI(2) – are used to create the redistributed contact pads on the top surface of a chip.

This desire to reduce the use of organic solvents led to the introduction of polybenzoxazole (PBO)-based dielectric materials. These were processed with an aqueous based developer, in fact, the same one used for photoresists. PBOs have similar properties to polyimides, but while they cannot hold up to high processing temperatures compared to polyimides, they tended to fully cure at lower temperatures and exhibited properties that helped RDL-packaged chips survive drop tests of handheld devices.

Taking fan out packaging beyond redistribution

As the demand for more and more features on electronic devices grows, the ICs have evolved into higher and higher functionality with more outputs. The ability to successfully redistribute a new layer of

continued on page 24

Toshiaki Itabashi, DuPont Semiconductor Fabrication Materials, Kanagawa, Japan

Redistribution and fan out *continued from page 22*

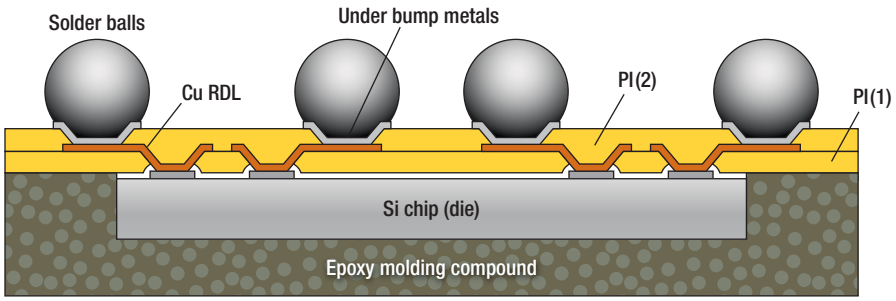

Figure 2. Polybenzoxazole (PBO) dielectric materials – shown as PI(1) and PI(2) – are used in fan-out packaging methods, because their lower curing temperature is compatible with epoxy packaging materials.

contacts over the surface of the chip reaches its practical limit with I/O counts above 200 contacts, due to the limited area available for placement of solder balls.

To increase the surface area available for solder ball placement, the chip can be embedded in a slightly larger epoxy frame, creating a technology called embedded wafer-level ball grid array (eWLB) [4]. In this case, the redistributed contacts cannot only be positioned over the chip but "fanned out" to the edges of the epoxy frame. The redistribution is accomplished in the same manner as before. A layer of dielectric material is applied to fill any gaps and smooth the surface across the chip and epoxy frame. The copper traces are applied next and they fan out across the entire surface area. A final dielectric layer covers the traces except where the solder balls will be placed.

As WLCSP packages have increased in I/O counts to >300, the current polymer dielectrics do not provide enough stress buffering to provide consistent reliability performance through drop and temperature cycle testing.

But while the redistribution process is similar, the new packaging scheme requires another evolution in dielectric materials. Because the frame is epoxy, it cannot survive the processing temperatures needed to cure polyimides or most PBO materials. Higher functioning ICs may incorporate embedded memory in the chip's design. This circuitry is very sensitive to process temperatures and survivability drops dramatically with increase in temperatures. In addition, advanced technology node wafers will use lower-k dielectric materials, which are themselves temperature sensitive.

Once again, the dielectric materials have had to keep up with the demands of the packaging technology, which is in turn, responding to the needs of the device designers. By modifying a PBO formulation, a new material has been developed that cures as low as 200°C. The trade-off is a reduction in the mechanical and chemical resistance properties of the dielectric, but work is underway to find a suite of process chemicals that will allow a robust process for volume manufacturing (**Fig. 2**).

What's ahead for dielectric materials?

As the semiconductor industry drives toward higher and higher data transfer speeds, 2.5D and 3D packaging schemes are being developed. In 2.5D packaging silicon interposers with through vias provide the interconnectivity. In pure 3D, the dies themselves have the vias and are stacked one upon the other. Both of these packaging structures use very thin (<50 micron) active dies that will require redistribution layers, adhesives and underfill materials. All these materials may require different mechanical, thermal and chemical properties than the incumbent products of today.

Work is underway developing these materials including: 1) the use of polyimide material as a temporary adhesive for bonding thinned wafers to a carrier wafer for processing; 2) a polyimide material as a permanent adhesive for bonding of wafer/chip stacks; 3) the use of a PBO dielectric material to bond backside circuitry onto thinned wafers (where the lower temperature curing is needed so as not to damage structures on the wafer); and 4) new over molding compounds for semiconductor packaging materials to help prevent die shift in fan out packaging.

Conclusion

According to John Hunt of ASE, as WLCSP packages have increased in I/O counts to greater than 300, the current polymer dielectrics do not provide enough stress buffering to provide consistent reliability performance through drop and temperature cycle testing. New polymers that are capable of buffering the die structures from the package stresses will be required, and once again materials will continue to evolve to meet the requirements of advances in packaging.

Acknowledgments

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ADVANCED SUBSTRATES

Planar fully depleted SOI: the technological solution against variability

EXECUTIVE OVERVIEW It is well known that the planar fully depleted silicon-on-insulator (SOI) (FDSOI) architecture is a technological booster of the CMOS performance, thanks to better electrostatics than devices on bulk. This article shows that it also greatly improves the variability of the electrical characteristics, thanks to an undoped channel. This leads to good matching performance.

The technology developed at CEA-Leti is illustrated by the transmission-electron-microscopy picture in **Fig. 1**. The thickness of the buried oxide (BOX) for our FDSOI devices is 145nm, 25nm or 10nm. The film thickness is ~7nm. Threshold voltages are adjusted by the gate-first work functions (targeted work functions are only ±150mV around the midgap). The technological details of the process integration, as well as the main recent results, are given in references [1-3].

This technology mainly addresses low-power applications, even if it is compatible with wafer-level or process-induced stressors for high performance [3]. In particular, it yields a 22% energy-consumption reduction at a given speed for ring oscillators at the 45nm node compared to the same circuit on bulk [1]. Other details about this technology, its performance and capabilities can be found in reference [4]. Finally, one of the main advantages of this technology is the low variability obtained.

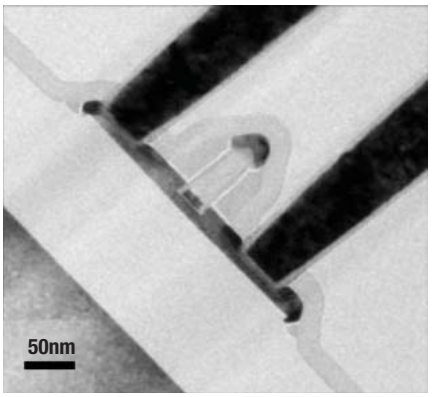

Figure 1. TEM image of a transistor on FDSOI with a T_{box}=145nm thick Buried Oxide (BOX), L=30nm gate length and a mesa isolation.

The variability issue and solution

For the 20nm CMOS technology node and below, the variability of the electrical characteristics is becoming as important as the electrical performances themselves. Especially, the threshold-voltage (V_T) variability is a key for the stability of the SRAMs, which represent a huge proportion of an integrated circuit area. Indeed, improving the V_T variability directly lowers the SRAM dispersions and, in turn, the minimal supply voltage (V_{DDmin}) of the memory blocks.

Historically, for CMOS on bulk, the dopant concentration in the channel of the transistors (N_{dop}) increases node after node (by a factor k) when the device dimensions (the active width W, the gate length L and the effective gate oxide thickness in the inversion regime T_{inv}) are scaled by a factor 1/k [5]. This scaling law is only based on electrostatic considerations and not on variability considerations. However, for sub-65nm CMOS, one of the most important showstoppers is the V_T variability, which is no longer negligible. Actually, the V_T standard deviation varies as $\sigma_{V_T N_{dop}} \propto T_{inv} \cdot \frac{\sqrt[4]{N_{dop}}}{\sqrt{W.L}}$ when it is limited by the random dopant fluctuation (RDF). This means that the intrinsic variability of CMOS on bulk theoretically degrades node after node (by a factor $k^{1/4}$). For the moment, the solution used by IC manufacturers to keep the V_T standard deviation of the nominal device quite constant with the scaling is not to play on the channel doping but to slow down the (gate length L and supply voltage V_{dd}) scaling or to counterbalance by electrostatic improvements (T_{inv} lowering or junction optimizations) or by design solutions. However, for the 20nm node and below, considerations on the dynamic power consumption require a V_{dd} scaling and electrostatic/performance considerations already require a challenging T_{inv}.

In this context, we propose another paradigm based on the planar FDSOI with undoped channels. In this architecture, the scaling is not governed by the channel doping but rather by the film thickness below the gate (T_{si}) [6]. This enables an excellent electrostatic behavior (better than CMOS on bulk) without any intentional channel doping. Such devices thus resist the root cause of the RDF (i.e., the channel doping) and simultaneously improve the electrostatics. Indeed, FDSOI is really an electrostatic booster, similar to the T_{inv} reduction. This enables a lower sensibility of the VT vs. the gate length (L) and, consequently, an additional reduction of the second major source of variability in bulk devices, namely line edge roughness (LER). This latter indeed influences the V_T standard deviation following:

$\sigma_{V_T,L} \propto \sigma_L \cdot \left(\frac{dV_T}{dL}\right)_{T_{inv},TSi,V_d}$ (σL being the effective channel-length fluctuation). Finally, the two major sources of variability (RDF and LER) are strongly or even completely reduced thanks to the FDSOI architecture. This is evidenced by **Fig. 2**, which shows that the LER-induced fluctuation (in blue and red) can be neglected compared to the "surface" sources of variability attributed to the gate stack

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(charge or gate work-function fluctuations), even down to L= 25nm.

Variability performance of FDSOI devices

Thanks to the undoped channel, we highlight a low variability, as evidenced by **Fig. 3** and [7]. It is worth noting that this performance was reproduced on FDSOI by another group [8]. It exceeds the one obtained on bulk devices or on FinFETs (not shown here). Indeed, for 3D devices and, contrarily, as for planar FDSOI architectures, V_T strongly depends on W. Thus, there is an additional contribution induced by the fluctuation of the fin width (W_{fin}), which is the smallest dimension of FinFETs:

$$\sigma_{V_T,W} \propto \sigma_{W_{fin}} \cdot \left(\frac{dV_T}{dW_{fin}}\right)_{T_{inv},T_{Si},V_d}$$

For planar FDSOI, however, SOI thickness (T_{Si}) is the smallest dimension. However, T_{si} is not defined by the lithography but rather by the Smart Cut process. This guaranties a very good process uniformity of T_{si}. We demonstrated that the T_{si} uniformity now reached by SOI wafer manufacturers (T_{si} range around 10Å [2][7]) is in the specifications for the 20nm node.

We checked that this outstanding variability performance is conserved in the following cases:

- With the introduction of mechanical stressors [7][9]
- With either 145nm thick or 10nm thin BOX [2]
- With or without back-biasing the substrate below the BOX

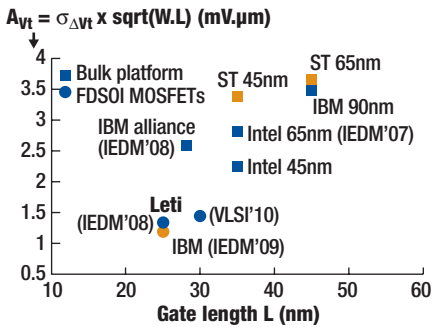

Figure 3. Benchmark of the matching factor vs. the gate length for bulk or FDSOI devices [7,8].

Finally, it must be stressed that the aforementioned local variability (namely the matching or the statistical variability) is the major part of the total variability over the whole wafer. The other part is the systematic variability. With systematic variability only, the electrical performances of all the devices on all the dies would be well known, modeled and mastered (by the process and the design). With local variability, the performances are not known; only the random distribution of performances is known. FDSOI architecture is the technological solution to minimize this uncertainty in order to proceed with the CMOS scaling.

Conclusion

To summarize, FDSOI technology exhibits outstanding variability results, thanks to the use of an undoped channel, and to the good control of silicon film thickness already reached today on commercial SOI wafers. Therefore, variability performance is much better than for planar bulk technology, for which variability is governed by random dopant fluctuation within the channel, and much than for FinFETs, for which the fin width fluctuation is the limiting parameter. This constitutes a key advantage of FDSOI technology, which offers today the only viable solution for scaling the supply voltage; it therefore keeps the circuit power consumption under control for the sub-20nm technology generations.

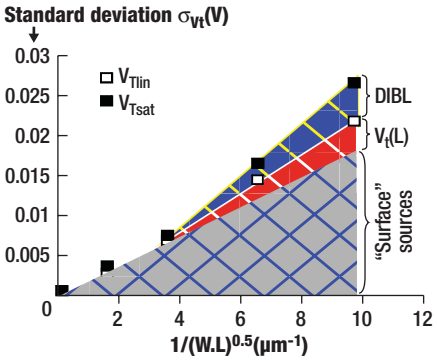

Figure 2. Pelgrom plot with V_T measured in the linear and in the saturation regime for T_{Si}=8nm.

Acknowledgment

SmartCut is a trademark of Soitec. ■

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Olivier Faynot is senior scientist and manager of the Innovative Device Laboratory at CEA-Leti.

PRODUCT NEWS

22nm, early-EUV photomask inspection

The Aera3 third-generation mask inspection system emulates the optical system of the lithography scanner, allowing users to immediately see if a defect will cause problems or can safely be ignored. Detection sensitivity is 50% improved vs. the previous Aera2 system; the system also features a more powerful light source (193nm) and smaller pixel size (67nm). An optional EUV module can detect defects as small as 12nm. **Applied Materials**, *Santa Clara, CA; 408/563-0647, www.appliedmaterials.com.*

Photomask registration

The PROVE system offers in-die photomask registration and overlay metrology for 193nm lithography. Autofocus and calibration enables <0.5nm repeatability and <1nm accuracy, working with NA=0.6 for greater depth-of-focus and large working distance. It measures local registration errors in areas where registration markers cannot be placed, and eliminates required marker space to increase useable mask areas. Individual masks are measured relative to design, with results superimposed to extract resulting local overlay error. **Carl Zeiss SMT AG**, *Jena, Germany; +49/3641-64-2242, www.smt/zeiss.com/sms.*

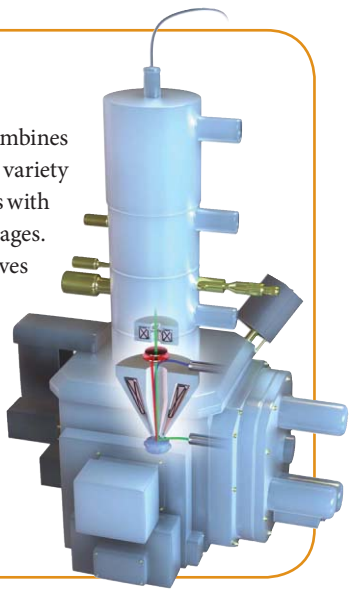
CMP polishing pads

The VisionPad 6000 is designed to improve defectivity and dishing for interlayer dielectrics and Cu bulk applications. A low-defect and low-hardness polymer chemistry and optimized pore size exceed removal rates of the IC1000 polishing pads—the company claims customer tests show 50%-60% reduction in scratch defects and 35% reduction in dishing, with equivalent nonuniformity. VisionPad 5200 CMP polishing pads achieve 10%-30% increased removal rate for W, ILD, and Cu bulk processes and 10%-20% reduction in defectivity in W and Cu applications, with better dishing and erosion in W applications vs. the IC1000 pads. **Dow Electronic Materials**, *Newark, DE; 302/366-0500, www.dow.com.*

Thermal analysis software

The FloTHERM 3D computational fluid dynamics simulation software provides bottleneck and shortcut fields to help engineers identify where and why heat flow congestion occurs in electronic designs, and identifies thermal shortcuts to resolve the problems. Enhancements in FloTHERM 9 include XML model and geometry data

Ultrahigh-resolution SEM



The JSM-7001FTTLS LV scanning electron microscope combines an objective lens and detector technologies to image a wide variety of samples, including magnetic materials. In-lens detectors with energy filtering provide topography and Z contrast images. "Gentle Beam" technology reduces charging and improves resolution, signal-to-noise, and beam brightness, especially at low beam voltages (down to 100V). The system operates at low magnification (10X) with no distortion of the image or EBSD pattern. A low vacuum mode enables imaging of nonconductive samples at high kV and beam currents. An optional STEM detector allows imaging of thin samples with sub-0.8nm resolution. **JEOL**, *Peabody, MA; 978/536-2309, www.jeolusa.com.*

importing to enable integration into existing data flows, and a direct interface to Mentor Graphics' Expedition PCB design platform. **Mentor Graphics**, *Wilsonville, OR; 503/685-7000, www.mentor.com.*

Switch mainframes for semi test

These switch matrix mainframes (six-slot Model 707B and single-slot Model 708B) offer an embedded test script processor so test scripts can be executed within the

instrument, enabling faster connect-source-measure sequences, and a digital control platform that supports faster command-to-connect speeds—overall system throughput is improved by up to 40% without changing any code, the company claims. Features include an updated front panel interface to simplify tasks e.g. configuration management and switch pattern programming, and a choice of GBIP, LXI, or USB interface options. **Keithley Instruments**, *Cleveland, OH; 440/248-0400, www.keithley.com.*

Wafer-edge metrology, inspection

The Visedge CV300R-EP edge metrology and inspection tool provides a calibrated measurement of the wafer edge profile, including slope of the bevel on which the film edge may land. It offers simultaneous edge defect inspection and multilayer metrology in the near-edge and top bevel regions, as well as patterned areas (including partial die). Other capabilities include multichannel (specular, scatter, phase) defect imaging and binning in the near-edge, top/bottom bevel, and apex regions of the wafer; enhanced performance of low-contrast films; ability to detect buried edges in dielectric films; and a rotating optical head to eliminate "blind spots" and "stitching" errors. **KLA-Tencor**, *Milpitas, CA; 408/875-3000, www.kla-tencor.com.*

Dual-chamber CVD diamond reactor

The Model 665 hot-filament CVD dual-chamber diamond deposition reactor can accommodate up to 18 100mm-dia. substrates at a time, doubling the throughput of the previous Model 650 (1.1µm/hour) but at 40% lower cost. Process controller and associated electronics, gas distribution, and pressure (vacuum) control simultaneously serve the two chambers. The system uses existing recipes with only minor pump down/cooldown step-time modifications. Target markets are CMP pad conditioners and diamond-coated electrodes for water treatment, and development of higher-volume deposition equipment for diamond interlayers on semiconductor wafers. **sp3 Diamond Technologies**, *Santa Clara, CA; 408/492-0630, www.sp3inc.com.*

Magnetically levitated turbopumps

The HiPace M series offer high pumping speeds (300 l/s, 700 l/s and 800 l/s) and high compression ratios for all gases, optimized to run in all orientations with a low vibration signature. The pumps are rated Protection Class IP54 for harsh industrial environments. An intrinsically low dynamic magnetic field does not interfere with even the most sensitive equipment. An integrated electronic drive unit reduces the need for cabling and cable failure. Power consumption and run-up time also have been reduced. An optional sealing gas connection safeguards against particulate buildup and oxidizing gases. **Pfeiffer Vacuum**, *Nashua, NH; 408/956-2578 x309, www.pfeiffer-vacuum.com.*

TECHNOLOGY NEWS *continued from page 12*

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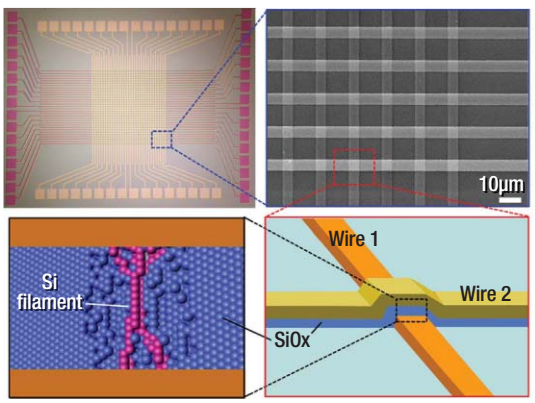
EUV mask data correction in less than eight hours on a single Tachyon system.

Accurate models across the full imaging field, as well as acceptable run times and file size, are key end user requirements, Jim Koonmen, GM of Brion, tells *SST*. But full-field is the key new requirement with EUV—and in turn, it drives acceptable run times and file sizes. The full-field nature of EUV makes the job more complex because the imaging performance can vary across the scanner's full imaging field. For example, flare (i.e., stray light) varies across the scanner's field. In immersion scanners, flare is insignificant. In EUVL, however, flare becomes a more substantial effect that is driven by attributes of the EUV mask and EUV scanner. These attributes lead to a nonhomogeneous distribution of flare across the imaging field, says Koonmen. If not dealt with appropriately, each chip in the imaging field may require its own unique correction, thereby exploding the data. Koonmen discusses how the new product addresses these challenges.

Brion says it will continue to invest in Tachyon NXE to continuously improve its capabilities, while developing a separate product that will enable customer access to NXE-specific effects within a broad range of simulation tools. This second product will be available soon. — ***D.V., J.M., M.C.***

At www.electroiq.com/podcasts.html, Jim Koonmen, GM of Brion, talks about the industry transition to EUV and the software's role. And Fujimura and SST's Debra Vogler talk about "making the impossible 80hr photomask possible." — J.M

Researchers: SiO_x OK for sub-10nm memory switch



Researchers at Rice U. say that a new switching memory they built with electrically manipulated 10nm graphite strips doesn't actually need the graphite—good ol' reliable silicon oxide will do just fine.

Last year a team led by Rice prof. James Tour showed that electrical current could break and reconnect graphite strips, creating a memory bit. Now, grad student Jun Yao shows in a *Nano Letters* paper that the same thing can be achieved with silicon oxide between semiconducting sheets of polycrystalline silicon (as top/bottom electrodes); applying a charge forms a chain of nanosized silicon crystals—as small as 5nm—which can be repeatedly broken and reconnected by varying the voltage. As a proof of concept, he cut a carbon nanotube to localize the switching site, sliced out a thin piece of silicon oxide with focused ion beam, and identified a nanoscale silicon pathway under a transmission electron microscope.

Silicon oxide switches or memory locations require only two terminals, not three (flash memory) because the device doesn't have to hold a charge. It also can be stacked in 3D arrays (which is the direction memory is going) and would be compatible with conventional CMOS manufacturing technology. And while there are questions about the future of conventional memory below 2Xnm, "our technique is perfectly suited for sub-10nm circuits," Tour said in a statement. These SiO_x circuits offer similar specs as the original graphite device: high on-off ratios, "excellent" endurance, and <100ns switching. They're also radiation-resistant, so they're also suitable for defense/aerospace radiation-hardened applications.

Austin design firm Privatran is bench-testing one of these silicon-oxide chips with 1000 memory elements, in work supported by a number of federal groups (NSF and the science arms of the Army, Air Force, and Navy). And a Rice spinoff company, NuPGA, is using vertical silicon oxide embedded in vias for rewritable gate array designs. — ***J.M.***

TECHNOLOGY NEWS *continued from page 12*

Sarah Okada of Strasbaugh gave an overview of the company's STB P300 polisher, touted as a customized solution for GMR polishing needs. The platform supports all substrate sizes from 125mm to 300mm. One GMR-unique feature is an option for rapid grinding of thick Al_2O_3 with 800 or 1200 grit abrasive as a rapid removal step before polishing the final 1-2µm.

Vamsi Velidandla of Zeta Instruments described a new 3D imaging and metrology microscope that builds up topographical images with 70nm vertical resolution using a broadband white-light LED source. Sample scans of polishing pads and pad conditioners showed a level of detail superior to other methods I've seen. The data sets included a black felt carrier pad, which is often impossible to measure by other optical methods because the reflection intensity is so low.

Denise Hunter of Cabot Microelectronics wrapped up the meeting with a description of their mixed abrasive slurry for HDD substrates. The NiP plated platters are typically smoothed in a two-step process: alumina abrasive coarse polishing followed by silica abrasive final polish. The irregularly shaped alumina particles can leave embedded fragments in the NiP grain boundaries, resulting in defects on the platter. The HDD mixed abrasive slurry combines alumina with much smaller colloidal silica abrasive. The silica is thought to envelop the alumina particles and decrease the incidence of fragmentation. Removal rate of the mixed abrasive slurry is ~10% lower than alumina slurry, but defect levels are significantly improved—to the extent that several HDD fabs are qualifying the new material for volume production. — ***Michael A. Fury Ph.D, senior technology analyst, Techcet Group***

AD INDEX

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INDUSTRY FORUM

OEM-level offsite outsourcing: a new paradigm

Robert de Neve, *E Systems Technology, Mountain View, CA USA*

For over 20 years, semiconductor original equipment manufacturers (OEMs) have outsourced the production of their equipment to offshore contract manufacturers (CMs) in an attempt to leverage the lower operating costs of the region and improve their proximity to their end user customers. As cost, communication, and logistics problems have increased, OEMs have been rethinking this strategy, however, and searching for alternative sourcing solutions. Add to this the increasing complexity of OEM products and concerns about intellectual property (IP) theft, and you have increasing demand for an entirely new approach to outsourcing; one that focuses on increased technical competency and IP protection.

What's needed is a new approach to sourcing and a new type of OEM supplier, one that departs from the current model of CM-based offshore outsourcing to a new paradigm of OEM-level offsite outsourcing that integrates ALL of the above functions into a single, low cost, high quality "Made-in-the-USA" solution for OEMs in the semiconductor equipment industry. This new paradigm must include the following elements: OEM-level capability, IP protection, and product life-cycle protocols.

As new OEM products become more complex, the need for OEM suppliers to provide highly technical solutions increases considerably. Traditional CMs fall short when product management, critical component sourcing, and systems integration services are required. This is because CMs are service-based companies with little or no product development and management experience; the very capability today's OEMs require from these suppliers.

OEMs wedded to the offshore approach to outsourcing battle a wide variety of competitive and IP-related problems. Having to send engineers out to the traditional CM to offset the supplier's lack of product-based skills is a prime example. This has negative effects on the OEM in terms of lost opportunity cost when engineers spend more time on supplier development than product development back at the factory. The risk of spawning new competition, if the supplier is located in a region where patent and IP laws are weak or non-existent, increases considerably as the CM can now take their new found skills and launch a competitive company.

OEMs wedded to the offshore approach to outsourcing battle a wide variety of competitive and IP-related problems.

A new CM paradigm is clearly required. PLC-based manufacturing strives to solve the current problems faced by OEMs looking to keep IP safe, costs down and quality up as they build ever more complex systems. PLC manufacturing is next in a long line of production system paradigm shifts, from craft-based production in England, to mass production as pioneered by Henry Ford in the U.S., to the much vaunted lean manufacturing techniques developed by the Toyota Production System. The strength and value of PLC manufacturing allows the supplier to apply sourcing, engineering, and manufacturing solutions based on the status of the OEM's product within the PLC. In other words, whether the OEM's product is in the early life (pre-release), mid-life (released), or late life (post-release) phase of the life cycle, the PLC-based manufacturing system has an appropriate solution. Leveraging suppliers with OEM experience and PLC compatibility helps the OEM mitigate risk and maximize product performance.

The power of PLC manufacturing lies in its ability to adapt to the needs of the OEM and interface with the in-house product development and operating systems, while providing IP security and guaranteeing the OEM that cost, quality, delivery and support requirements are met. PLC manufacturing and OEM-capable suppliers are a new approach to contract manufacturing as defined by OEMs *for* OEMs. ■

Robert de Neve is president & CEO of *E Systems Technology, 1305 Terra Bella Ave., Mountain View, CA 94043 USA; 650.961.0671 email rdeneve@esystems technology.com.*

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