

Solid State TECHNOLOGY®

Insights for Electronics Manufacturing

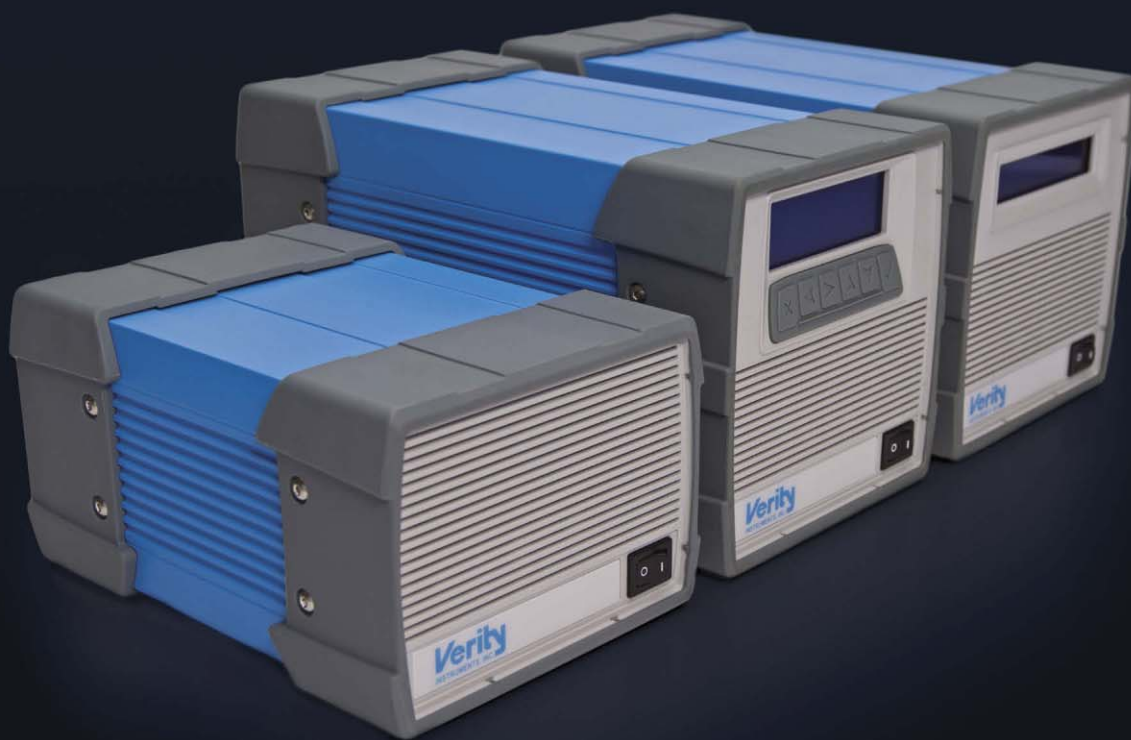
**New Materials for
Displays** P. 17

**Testing Complex
Probe Cards** P. 20

**Defects in 3D Die
Stacks** P. 24

**BCDMOS
for 700V
Driver Chips** P. 14

We've gone the extra mile so you don't go the extra nanometer.



THE NEXT GENERATION HAS ARRIVED.

Introducing the latest additions to the Verity family of smart spectrometers featuring the SD1024X, a new industry standard that combines spectrometer and PC in the same space, eliminating the need for a dedicated applications computer. The new SD1024G Series delivers improved capability with industry leading ultra-performance, general purpose, and high resolution model options. Coupled with the compact FL2100 flashlamp module the new series addresses the broadest range of challenging plasma and film thickness/etch depth endpoint control problems. Now, more than ever, the first name in endpoint detection is the last word in performance.

Learn more at www.Verityinst.com.

Verity

INSTRUMENTS, INC.

Solid State TECHNOLOGY®

Insights for Electronics Manufacturing

New Materials for
Displays P. 17

Testing Complex
Probe Cards P. 20

Defects in 3D Die
Stacks P. 24

BCDMOS
for 700V
Driver Chips P. 14



Solid State Equipment LLC

ADVANCED PACKAGING
SINGLE WAFER
WET PROCESSING



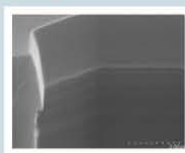
TSV RESIST STRIP AND CLEAN



As received - post DRIE



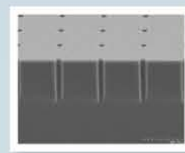
After SSEC Cleaning



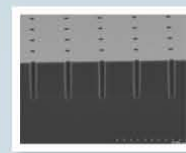
As received - post DRIE



After SSEC Cleaning

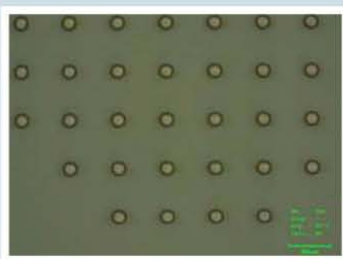


As received - post DRIE

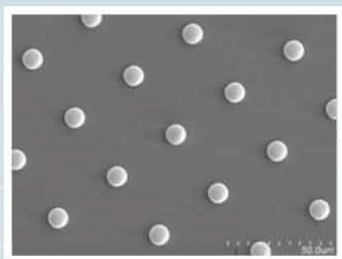


After SSEC Cleaning

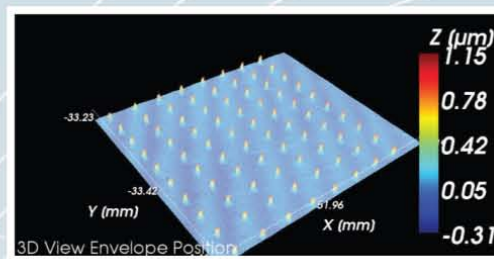
Si ETCH TO REVEAL Cu TSV



Optical

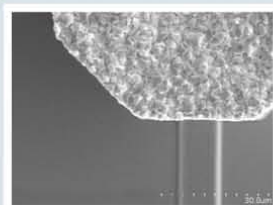
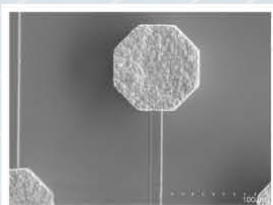
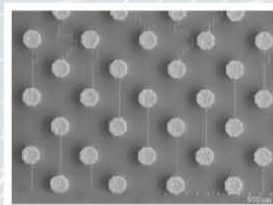
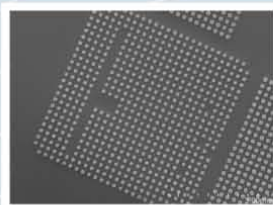


SEM

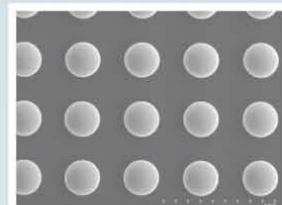


ISIS 3D

DRY FILM STRIP



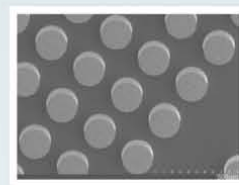
FLUX CLEANING



UBM AND RDL METAL ETCH



UBM Post Etch



UBM Post Strip

ssecusa.com

© 2012 SOLID STATE EQUIPMENT LLC



Solid State TECHNOLOGY®

SEPTEMBER 2012 VOL. 55 | NO. 7

An employee testing a wafer at Dongbu HiTek's Fab 2 in Sangwoo, Korea.

COVER

FEATURES

14

HIGH VOLTAGE DRIVERS | BCDMOS designed for 700V driver chips

A specialized ultra high voltage BCDMOS process at the 0.35 μ m node deploys thin n-epitaxial technology to support high voltage applications. *Jae Song, Dongbu HiTek, Seoul Korea.*

17

DISPLAYS | Material support: helping displays deliver higher performance

Metal oxide transistors increase electron mobility by a factor of up to 40 compared to conventional technology, at a comparable cost base. *Andreas Weisheit, Linde, Shanghai, China, and Greg Shuttleworth, Linde, Guildford, UK.*

20

TEST | Testing probe cards that contain complex circuitry

State based testing is a simple, highly scalable method to describe activation details for probe card circuitry. *Greg Olmstead and Bob Davis, Rudolph Technologies, Inc., Flanders, NJ.*

24

PACKAGING | Defect detection in die stacks with acoustic imaging

A new simulation technique makes imaging easier and faster for stacked die and other multi-layered structures. *Tom Adams, Sonoscan, Inc., Elk Grove Village, IL.*

27

Lithography | Understanding shape-dependent mask CD uniformity

Process development teams will need to consider the impact of shape-dependent mask CD uniformity on design rules and wafer yields *Aki Fujimura, D2S, Inc., San Jose, CA*

COLUMNS

- 3 **Editorial** | A new era for suppliers, *Pete Singer, Editor-in-Chief*
- 12 **Packaging** | Advances in wafer underfill processing, *Dr. Phil Garrou, Contributing Editor*
- 13 **LEDs** | Wafer bonding enables better LEDs, *Thomas Uhrmann, EV Group*
- 32 **Industry Forum** | Nanoimprint lithography's role in 450nm, *Paul Hofemann, Molecular Imprints*

DEPARTMENTS

- 2 Web Exclusives
- 6 News
- 31 Ad Index

online@ www.solid-state.com

Web Exclusives

System architecture + anthropology = Better sensor algorithms

Ian Chen, Sensor Platforms, discusses the role of sensors in smart devices, evolving from pure metrological instruments to context-aware user assistance devices. Key points include sensor fusion with data input and algorithms, and power consumption control. <http://bit.ly/QQPitW>

Terry Brewer chats about SEMI, semis at SEMICON West

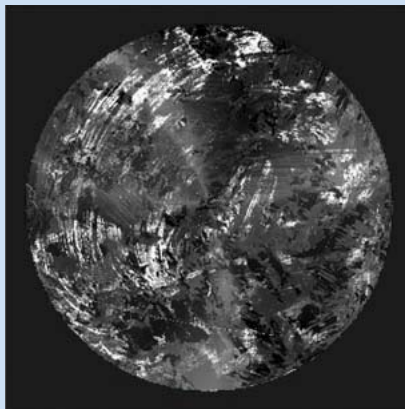
Terry Brewer, the newest member of the SEMI North American advisory board, talks about semiconductor industry consolidation, as well as new technologies and materials in the industry. <http://bit.ly/Mmqd8e>

LED insights from SEMICON West

Citi analysts surveyed the LED manufacturing market and demand at SEMICON West, including a slight uptick in MOCVD orders, and some backlash against Cree's downstream ambitions. <http://bit.ly/MCgVzj>

Process Watch: Bigger and better wafers

In the third installment of Process Watch, the authors discuss some of the challenges of metrology on 450mm wafers. Authored by experts at KLA-Tencor, Process Watch articles focus on novel process control solutions. <http://bit.ly/OueEe7>



n&b news and blogs

How fabless works for MEMS with InvenSense

Joseph Jiang, InvenSense, spoke with us about their fabless approach to MEMS innovation and its NF-Shuttle, which launched in 2012 and will do a third run. <http://bit.ly/OkEHS8>

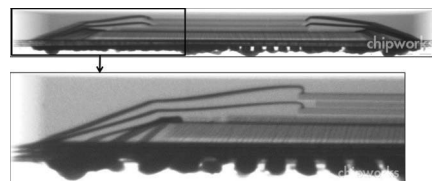
Where has the love of MEMS gone?

Karen Lightman, MEMS Industry Group, asks, "Has the romance between the MEMS and semi industries started to fizzle?" <http://bit.ly/ME2z3w>

Samsung breaks 3D IC wall of silence at DAC 2012

Samsung, who has been on absolute lockdown when it comes to 3DIC materials leaking out of the company, opened the door... just a little bit. Dr. Phil Garrou reports. <http://bit.ly/Rfng8N>

Sony PS Vita used 3D packaging, or does it?



In a teardown of Sony's Vita, Dick James, Chipworks, found an interesting die-stack package: "Stacked Chip SoC." <http://bit.ly/M1DRr0>

Vacuum *Pressure Measurement*



Residual Gas Analyzers

- 100, 200 and 300 amu models
- Sensitivity to 5×10^{-14} Torr
- Dual ThO_2Ir filament
- Long-lasting electron multiplier
- 6 decades of dynamic range
- Windows software

RGAs starting at \$3750

Ion Gauge Controller

- 1000 Torr to UHV range
- 0.3 % controller accuracy
- Touch-screen display
- Pressure vs. time curves
- 8 channel process control
- 4 analog I/O ports
- RS-232, GPIB and Ethernet

IGC100 starting at \$1495

The SRS line of Residual Gas Analyzers and Ion Gauge Controllers are designed to meet virtually any vacuum pressure measurement need.

The IGC100 Ion Gauge Controller monitors total pressure from up to two ion gauges, two convection enhanced Pirani gauges and four capacitance manometers. There's a touchscreen display that shows gauge pressures in large, easy to read numbers. You can also graphically display pressure vs. time curves. In addition, the IGC100 has an optional ethernet port for web interfacing.

RGAs from SRS bring large dynamic range, high resolution and excellent linearity to partial pressure measurements. A dual ThO_2Ir filament and unique four channel electron multiplier extend operating life. Windows control and analysis software along with an RS-232 interface is provided at no charge.

Prices are U.S. list



Stanford Research Systems

1290-D Reamwood Ave.
Sunnyvale, CA 94089
Phone (408) 744-9040
Fax (408) 744-9049
email: info@thinkSRS.com
www.thinkSRS.com



editorial

A new era for equipment suppliers

The semiconductor equipment industry received quite a jolt recently. In July, lithography equipment supplier ASML announced a "customer co-investment" program that enabled minority equity investments in ASML (up to 25% total) by its largest customers. Customers could also make commitments to fund ASML's research and development (R&D) spending for future programs.

Intel was the first investor, acquiring 15% equity ownership interest in ASML. R&D funding and equity investment agreements totaled approximately \$4.1 billion. Part of the deal was a contractual commitment from Intel for advance purchase orders for 450 mm and EUV development and production tools from ASML. ASML has said the results of the technology

ASML's R&D programs.

The Intel announcement made instant believers out of many that both EUV and 450mm would actually happen. Both technologies have been significantly delayed beyond initial target dates, and the thinking was that some massive investment would be required to get them production-ready in a reasonable timeframe (i.e., 2015-2020). \$5+ billion is a pretty good start!

Not only does it seem to ensure that EUV will succeed, but it removed one of the most significant barriers to 450mm development. Even if 450mm solutions were developed for all the other types of process equipment – deposition, etch, ion implant, CMP, cleaning, etc. – it would be going nowhere without EUV. Now, seemingly overnight, 450mm seems inevitable.

It is a new era for semiconductor manufacturing equipment suppliers, for they must now seriously tackle the 450mm challenge... but don't expect a blossoming new model based on customer co-investments anytime soon. There are at least two competitors in other markets, and developments will likely be funded the way they always have been – though good old-fashioned capitalism.

—Pete Singer, Editor-in-Chief

Intel made instant believers out of many that both EUV and 450mm would actually happen

investments will be available to every semiconductor manufacturer with no restrictions.

In August, TSMC joined in, taking a 5% stake in ASML, worth about \$1.04 billion. TSMC also committed about \$341 million, spread over 5 years, to

Solid State TECHNOLOGY

Susan Smith, Group Publisher
Ph: 603/891-9447, susans@pennwell.com

Pete Singer, Editor-in-Chief
Ph: 603/891-9217, psinger@pennwell.com

Meredith Courtemanche,
Editor, Digital Media Ph: 603/891-9176,
mcourtemanche@pennwell.com

Robert C. Haavind, Editor-at-Large
Ph: 603/891-9453, bobh@pennwell.com

Phil Garrou, Contributing Editor

Michael Fury, Contributing Editor

Justine Eversman, Marketing Manager

Cindy Chamberlin, Presentation Editor

Katie Noftsgger, Production Manager

Dan Rodd, Illustrator

Debbie Bouley, Audience Development

Marcella Hanson, Ad Traffic Manager

EDITORIAL ADVISORY BOARD

John O. Borland, J.O.B. Technologies

Michael A. Fury, The Techcoet Group, LLC

Rajarao Jammy, SEMATECH

William Kroll, Matheson Tri-Gas

Ernest Levine, Albany NanoTech

Lars Liebmann, IBM Corp.

Dipu Pramanik, Cadence

Design Systems Inc.

Griff Resor, Resor Associates

A.C. Tobey, ACT International

EDITORIAL OFFICES

PennWell Corporation,
Solid State Technology
98 Spit Brook Road LL-1,
Nashua, NH 03062-5737;
Tel: 603/891-0123; Fax: 603/891-0597;
www.ElectrolQ.com



CORPORATE OFFICERS

1421 South Sheridan Rd., Tulsa, Ok 74112
Tel: 918/835-3161

Frank T. Lauinger, Chairman

Robert F. Biolchini, President and CEO

Mark Wilmoth, Chief Financial Officer

TECHNOLOGY GROUP

Christine A. Shaw, Senior Vice President
and Publishing Director

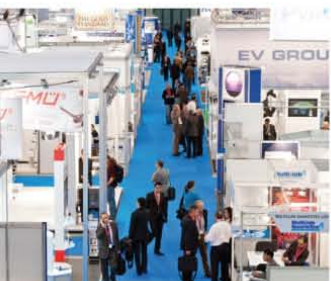
For subscription inquiries:

Tel: (847) 559-7500; Fax: (847) 291-4816;
Customer Service e-mail: sst@omeda.com;
Subscribe: www.sst-subscribe.com

We make portions of our subscriber list available to carefully screened companies that offer products and services that may be important for your work. If you do not want to receive those offers and/or information, please let us know by contacting us at List Services, Solid State Technology, 98 Spit Brook Road, Nashua, NH 03062. All rights reserved. No part of this publication may be produced or transmitted in any form or by any means, electronic or mechanical, including photocopying, recording, or by any information storage retrieval system, without written permission of the copyright owner. Prices for bulk reprints of articles available on request. Solid State Technology articles are indexed in Engineering Information and Current Contents, and Applied Science & Technology Index and abstracted by Applied Science & Technology Abstracts.



The Power of [x]

SEMICON®
Europa2012

The Power of [Europe]

9–11 October
Messe Dresden, GermanyEUV
LED/SSL
450mm
More than Moore
[Europe]
3D IC
MEMS
Fab Automation
Equipment

Connect to the trends, technologies and people driving the European Semiconductor Industry forward.

SEMICON Europa is the place to see the leading companies, technologies, and people driving the future of micro- and nanoelectronics design and manufacturing.

SEMICON Europa exhibitors are the suppliers to and partners of Europe's leading microelectronics companies. From silicon to system – and everything in between and beyond – SEMICON Europa showcases the biggest and brightest names in microelectronics manufacturing.

Plan now to be part of
SEMICON Europa 2012
www.semicon.europa.org

SEMICON Europa Programs:

- 14th European Manufacturing Test Conference (EMTC)
- Advanced Packaging Conference
- 16th Fab Managers Forum
- International MEMS / MST Industry Forum
- 6th Executive Summit
- SEMI Market Briefing
- Metrology, Process Control, Automation and Software Session
- 3D IC Session
- Power Electronics Session
- Secondary Equipment and Technology Session
- LED / SSL Session
- Workshop on Equipment Assessment & Performance Improvements
- Standards Meetings

Co-located with:

**PE 2012** EXHIBITION & CONFERENCEwww.plastic-electronics.org

Please send news articles to
meredithc@pennwell.com

news

worldnews

US | A federal court jury found that **Toshiba Corporation** and its subsidiaries conspired with the world's other leading manufacturers of TFT-LCDs to raise and fix the prices of TFT-LCD panels and certain products, awarding a total \$261 million charge against Toshiba. <http://bit.ly/NaL0c1>

US | **ST** acquired the IP of start-up **bTendo**, and hired the staff, following a joint development effort with the laser technology company. <http://bit.ly/OFngf2>

EUROPE | **Movea**, motion processing and data fusion technology developer, raised EUR6.5 million in a funding round led by **Intel Capital**. <http://bit.ly/Qyegy5>

ASIA | **UMC** gained LEED-NC Gold recognition for its eco-friendly 300mm Fab 12A P3 & P4 in Taiwan. UMC's P5 & P6 will also be green. <http://bit.ly/QwovA9>

ASIA | **Toshiba** will start mass production of white GaN-on-Si LEDs on a new 200mm wafer production line in its Kaga Toshiba Electronics Corporation fab in northern Japan. <http://bit.ly/N7U5QH>

US | **GLOBALFOUNDRIES** approved plans to expand its Fab 8 in NY, adding 90,000 more square feet of semiconductor manufacturing space in Module 1. <http://bit.ly/Nb4JM5>

US | **Goodrich** added 46,00sq.ft. to its high-tech manufacturing facility in Burnsville, MN, with areas for MEMS design and production. <http://bit.ly/MJldpr>

EUROPE | Germany launched a project, EUV projection optics for 14nm resolution, or ETIK, led by Carl Zeiss. <http://bit.ly/TfV3yK>

imec plans 450mm cleanroom with govern

imec will build a 450mm wafer fab cleanroom at the research organization's site in Belgium, with a new EUR100 million government investment, announced by the Flemish Minister of Innovation Ingrid Lieten. *Solid State Technology* caught up with Luc Van den hove, president and CEO, to discuss the implications for semiconductor manufacturing at 450mm, how to build a 450mm-capable cleanroom, and more.

imec's aim is to provide research 2-3 nodes ahead of what is in the semiconductor production fabs today, which means imec is working on process challenges, throughput enhancement, etc, for the 10nm/14nm node. The transition to larger 450mm wafers will coincide with moves to this smaller

process node, and both changes will affect manufacturing greatly, Van den hove said. "With each step in the process, there will be specific challenges when you convert to 450mm," he said. Throughput must be high enough to reap the benefits of the larger wafer size.

Initial 450mm assessment is taking place now, with R&D on processes slated to occur in 2015 and 2016. Early manufacturing will begin in 2017. With this in mind, imec recognized a need to open the new cleanroom by mid-2015. Initial tool assessments will be done in the 450mm-compatible area of imec's 300mm pilot line cleanroom.

What goes into making a cleanroom 450mm accessible? Higher ceilings, increased weight-bearing specifications, and more room for

Printed electronics standards initiative starts with substrate materials

IPC — Association Connecting Electronics Industries and JPCA (Japan Electronics Packaging and Circuits Association) released their first operational-level standard for the printed electronics industry, IPC/JPCA-4921, Requirements for Printed Electronics Base Materials (Substrates). The standard defines terms and establishes basic requirements for substrate materials used in printed electronics: ceramic, organic, metal, glass and other.

Printed electronics is still in its infancy, with commercialization spurts and lacking standard manufacturing practices. Printed electronics are generally made with long-established technologies combined with recent innovations, IPC and JPCA point out. Electronics can be printed on diverse materials, which both opens new opportunities and limits growth/targeted development programs. "It's difficult to grasp

Continued on page 10

ment investment

tools like EUV lithography scanners, said Van den hove. The equipment will require new wafer stages that move at high speeds through various environments (air, liquid, etc).

imec will also bolster its metrology suite to evaluate 450mm/1Xnm node processes, with a focus on perfect layer uniformity across the larger wafer surface.

The EUR100 million investment will help imec extend 450mm wafer development investments to EUR1 billion in the next 5 years, when the researchers will be installing 450mm tools and equipment. imec is negotiating the investment with the European Commission for funding and with global industrial partners such as foundries and fabless/fablite semiconductor companies, as well as semiconductor manufacturing equipment and materials suppliers.

The government's return on its investment is a high-tech ecosystem in Belgium, and Europe as a whole, Van den hove said. Semiconductor manufacturing tool suppliers need to invest a large sum in 450mm development, and they are looking for support from other parties to lessen this burden. Many of the major tool and materials suppliers for chipmaking are based in Europe, as are many fabless semiconductor companies. Government investment like that announced today fosters an "innovation engine" in Europe, Van den hove concluded. —M.C

www.solid-state.com

Semiconductor Assembly

Andy C. Mackie
PhD, MSc
Global Product Manager
amackie@indium.com



Visit my semiconductor blog for the latest on:

- 2.5D and 3D fluxes
- Package-on-package
- Pb-free power semiconductor solders



Learn more:
<http://indium.us/E024>

From One Engineer To Another®

www.indium.com/solar
solarteam@indium.com



.....
ASIA • CHINA • EUROPE • USA
.....

©2012 Indium Corporation

newscont.

SEMICON West hosts 2012 ITRS updates

2012 is an even-number year, meaning that only updates, rather than major revisions, are made to the International Technology Roadmap for Semiconductors (ITRS). At SEMICON West, ITRS reps presented 2012 changes and guidance on expected revisions in 2013.

For front-end semiconductor manufacturing, expect increased device density through new transistor architectures (strain, high-k metal gate and now the new multi-gate FET). The targets for dimensional scaling and the power/performance management of leading devices, are set primarily by gate length in conjunction with equivalent scaling.

New work is also being done to address max on-chip frequency. The transition to 450mm wafers is also an active research area in the US and Europe. ITRS has moved the forecast production start date to 2015-2016.

In the back-end assembly arena and "More than Moore" technologies, MEMS sensor integration is a hot topic, with sensors going from stand-alone devices to integrated 6-, 9-, and 10-degrees of freedom (DOF) devices. 3D and 2.5D interposer packaging are both front-of-mind for ITRS working groups as well. ITRS is adopting an application-driven roadmapping model for some of the new device technologies in semiconductors.

In single-chip packaging areas, the focus is primarily on lowering costs. For 3D packaging, ITRS is looking at roadblocks such as thinned wafer/die handling and high-volume TSV fabrication.

On the photonics integration question, ITRS still has a lot of "bricks" — items on the roadmap flagged red to indicate that the industry does not know how to tackle a challenge — and even more yellows — areas where the industry is not sure if a technology will work. —M.C

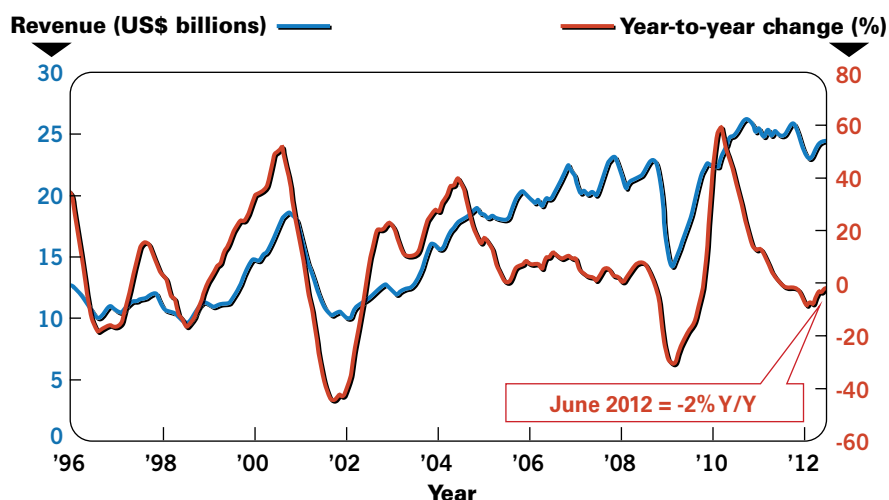
Chipmakers see a flat future in H2

Reporting Q2 numbers and issuing Q3 guidance, chipmakers like ON Semiconductor Corporation (Nasdaq: ONNN), Texas Instruments Incorporated (TI, NASDAQ:TXN), STMicroelectronics (ST, NYSE:STM), AMD (NYSE:AMD), and Intel Corporation (NASDAQ:INTC) consistently reported flat or lowered guidance, citing macro economic conditions.

- ONNN will be looking for a new CFO, with Donald Colvin vacating the post within 90 days. ONNN also authorized its first share repurchase program. <http://bit.ly/MLD1ke>
- Fab under-absorption charges will weigh on TI in Q3 and into Q4, analysts point out. <http://bit.ly/Oe0Y3K>
- ST said it will reduce its 2012 capex plan by about 25%, down to \$500 million to \$600 million. <http://bit.ly/NUNwoi>
- AMD reported lower channel demand for AMD desktop processors in China and Europe. <http://bit.ly/O0JjRF>
- Intel still expects a solid 2012, despite softer demand and a lower Q3 guidance, partly due to downstream supply chain participants managing inventories leaner ahead of the Win8 ramp in 4Q12. <http://bit.ly/S1eRDq>
- Following basically flat FYQ3 revenue and outlook for Q4 flat to down slightly, Infineon froze headcount and sharply reduced investments planned for FY2013. <http://bit.ly/P81moE>
- Qualcomm Incorporated (Nasdaq:QCOM) says growth estimates are now moderated to be "more back-end loaded," with a lower outlook for semiconductor volumes in FYQ4. QCOM is ramping 28nm chip supply, aiming for a strong December quarter. <http://bit.ly/Oe9eDh> —M.C

Flat chip sales in June, says SIA

Global semiconductor sales stayed flat in June 2012, hitting \$24.38 billion (a decline of 0.1% from May 2012), reports the Semiconductor Industry Association (SIA). Year-over-year (Y/Y), sales fell just 2% in June, a slower decline than the semiconductor industry has seen since October 2011.



Worldwide semiconductor revenues, Y/Y percent change. Source: WSTS

"The semiconductor industry continues to navigate the turbulent global economy better than most sectors, but macroeconomic uncertainties are limiting overall recovery and growth," said Brian Toohey, president & CEO, Semiconductor Industry Association.

"Congress can help ease economic uncertainty by enacting effective and dependable policies that promote American competitiveness and spur economic growth."

Regionally, semiconductor sales increased on a sequential monthly basis in Japan (2%) and Asia Pacific (0.6%) but declined in Europe (-0.7%) and the Americas (-3.6%).

Compared to June 2011, sales in June 2012 increased in Japan (3.7%) and Asia Pacific (1.0%) but fell steeply in the Americas (-8.1%) and Europe (-12.1%). "The Japan and Asia Pacific sequential increases are encouraging signs, but are tempered by continued weakness in Europe and the Americas," said Toohey.

This is the first time since September 2010 that Japan and Asia Pacific attained month-over-month and year-over-year growth simultaneously. —M.C

The New PRESTO®

Thermodynamic Power

Process Temperature
Control Solutions
for MOCVD, HB-LED



www.julabo.com

(800) 458-5226

Julabo
THE TEMPERATURE CONTROL COMPANY

newscont.

Apple out-buys all other semiconductor purchasers

Apple Inc. is not only the world's leading OEM in terms of semiconductor purchasing, its also is increasing semiconductor buying at a faster rate than other top firms, reports IHS.

Apple will buy nearly \$28 billion worth of semiconductors this year, up 15% from \$24 billion in 2011. Apple will dramatically out-buy Samsung Electronics Co. Ltd., its closest OEM competitor for semiconductor consumption. Apple took over the top spot in 2010. —M.C

TABLE. Top 10 OEM semiconductor buyers in 2012, ranked by purchasing revenue. (Revenue in \$B)

2012 Ranking	Company	2011	2012	2011/2012 Growth
1	Apple	24.3	28.0	15.1%
2	Samsung Electronics	14.8	14.9	0.3%
3	Hewlett-Packard	14.6	13.7	-6.5%
4	Dell	10.6	10.2	-4.2%
5	Sony	9.2	9.4	2.7%
6	Panasonic	9.1	8.8	-3.9%
7	Cisco Systems	8.8	8.4	-4.7%
8	Canon	7.3	7.6	4.6%
9	Toshiba	5.6	5.7	1.8%
10	Fujitsu	5.8	5.6	-3.6%

LED fab equipment capex to brighten in H2

Barclays Capital Inc. analysts held conversations with the LED supply chain at SEMICON West, confirming for Barclays that Q2 2012 orders for MOCVD tools remained flattish with the trough-like Q1 numbers.

Top MOCVD suppliers Veeco and Aixtron confirm that activity is picking up into H2 2012. Sub-component suppliers to the MOCVD makers, as well as

adjacent LED equipment suppliers, are anticipating gradual order growth in Q3 and Q4 2012.

Key accounts that are in the process or on the cusp of placing orders in the remainder of 2012 include Sanan and 3E in China, Toyoda Gosei and Showa Denko in Japan, a little bit of Epistar in Taiwan exiting the year, and likely Samsung in Q4 for equipment installation in 2013.

Additionally, Nichia also appears to be actively ramping capacity, though this will not benefit Veeco or Aixtron, given Nichia's internal tool production.

Barclays Capital estimates that MOCVD chamber shipments will pick up from 67 in H1 2012 to 80 in H2. The risk to MOCVD orders comes from the HDD sector, and how much it decelerates in H2, though service should provide a buffer here. —M.C

Continued from page 6

the breadth of opportunities when a range of materials can be printed onto various substrates to produce from very simple electronic circuits to the highly complex," said IPC Director of Technology Transfer Marc Carter.

For this technology to become a stand-alone industry, it must

have some commonalities that help build a structure, said Carter. The standard aims to provide a common language for designers, equipment makers and manufacturers.

IPC/JPCA-4921 provides a starting point for IPC's Printed Electronics Initiative to establish a critical segment of the infrastructure that will help

the industry expand more quickly. This initiative includes a dedicated management council for companies to discuss issues and to help develop tools and studies; a printed electronics conference track and exhibition area at IPC APEX EXPO 2013; and more industry standards, in continued partnership with JPCA.. —M.C

The energy behind energy at SEMICON West

At SEMICON West, keynoter Shekhar Y. Borkar, Intel Fellow and director of extreme-scale technologies at Intel, focused on the energy demands of ubiquitous computing, and how technologies developed for super computers will later be adopted into smartphones. The energy demands of today's transistors, Borkar says, will not be sustainable at the exaflop data rate. At CEA-Leti's presentations later that day, researchers agreed. So how can we achieve a new power consumption paradigm?

Different transistor-level technologies can address reducing power consumption. Borkar shared Intel's 22nm 3D trigate transistor and voltage scaling at the circuit level. Intel's trigate design reduces the required supply voltage and can be

tuned for different thresholds. Intel has developed an experimental processor to demonstrate this work.

Borkar discussed the use of SoC for targeted efficiency and flexibility — using single-purpose blocks that are energy efficient along with the flexible blocks, such as micro-processor, to make a chip accommodate various operations. Borkar calls this “valued performance.”

Other energy-saving options include stacking DRAM memory with a logic buffer to direct access to a specific page -- see the Hybrid Memory Cube -- and co-optimized circuits and interconnects.

At CEA-Leti's research meeting, Hughes Metras, VP of strategic partnerships in North America, also projected that the next step in super

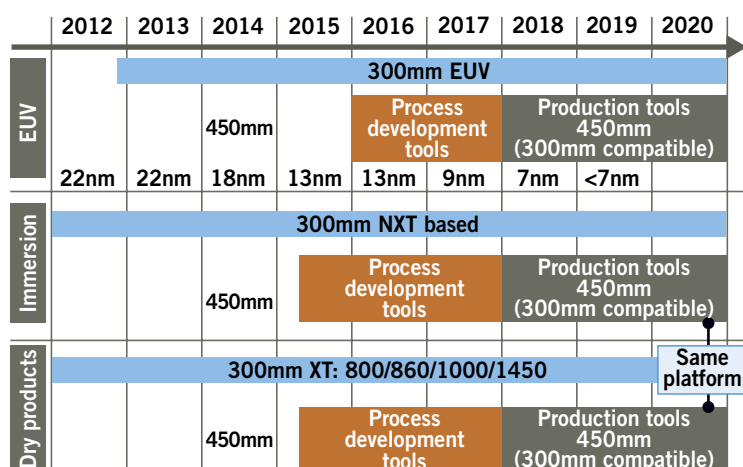
computing, exascale, would be insupportably energy intensive. Leti proposes planar FDSOI transistors, silicon photonics for light-based data communication, and 3D for lower-loss and shorter interconnects.

Maud Vinet, Leti assignee at IBM, focused on planar FDSOI transistors. We already have the majority of the wafer processing technologies we need for planar FDSOI in bulk CMOS. The biggest change is extremely thin Si films, adding importance to Si loss. The smaller gate lengths of planar FDSOI prevent parasitics, for faster operation. Back bias allows the device's threshold voltage to be tuned, a concept discussed during Intel's keynote as well. Planar FDSOI offers 30% less power dissipation than bulk transistors. —M.C

Intel, TSMC take stakes in ASML to push EUV, 450mm forward

ASML launched the ASML Holding N.V. Customer Co-Investment Program, wherein customers can take

up to 25% stake in the semiconductor manufacturing tool supplier, funding research primarily on EUV lithography and 450mm tools. Intel was the first taker,



ASML enhanced development roadmap.

grabbing 15% share and spending an additional EUR 829 million, over 5 years, on R&D at ASML. TSMC soon followed with a 5% stake in ASML and an additional EUR 276 million for R&D. Samsung is expected to be the target customer to take the 5% stake still available in ASML.

If the maximum aggregate 25% available shares are fully subscribed, customers would have acquired the shares for an aggregate value of EUR 4.19 billion, and would have committed R&D funding of EUR 1.38 billion, to be received over the period 2013 to 2017. —M.C

Advances in wafer underfill processing

At ECTC 2012, Toray presented results of their study on suppressing wafer level underfill (WUF) material entrapment at copper pillar/pad joints. The NCF (non-conductive film) was laminated on the wafer and then the surface was planarized by the bit cutting technique. Chips were then bonded to Cu/Ni/Au pads. When the top chip and lower chip are joined, the temp must be raised slightly (sticking process) to get the NCF to flow together. This holds the two chips in place.

Namics reported on the parameters controlling NCF performance. One of the main issues with NCF has been voiding. Namics reports that one of the causes of voids is captured air which is generated when an IC connects to NCF. This relates to the flow of resin. They could decrease the voids by optimizing the minimum melting viscosity. Another type of void comes from volatilization of gases, which may occur from organic materials in the structure such as the substrate. They found that the higher the minimum melting viscosity is, the more effectively these types of voids can be controlled. They also optimized the minimum melting viscosity, curability and flux-ability for good interconnection. When the minimum melting viscosity is too high, the connection is poor. When cure speed is too high, solder melting is blocked. They attempted to optimize flux activity, and found that gelling time, minimum melting viscosity and oxidation-reduction power need to be controlled.

Packaging



Hitachi Chemical (HC) also reported on their attempts to optimize their NCF products. HC said that the major requirements for processability are (1) NCF can be laminated to the bumped wafer without air-trapping around the bumps and dicing lines; (2) In the process of back grinding, the wafer laminated with NCF can be back-grinded (opposite side of NCF) to a thinner wafer without damage such as wafer crack and delamination of the NCF; (3) the alignment mark or dicing pattern on the wafer can be recognized through the NCF; (4) the NCF-laminated wafer can be diced without damage such as chip crack and delamination of the NCF.

Hitachi Chemical (HC) reported on their studies on using solid molding compounds for fan out WLP and molded underfill (MUF). Currently, liquid molding compounds are mainly used for eWLB as encapsulants. Liquid molding compound issues include cost, warpage and high die stand-off caused by molding shrinkage.

Koyanagi-san and co-workers at Tohoku University have looked at the issue of NCF and compression molding for 3D integration using self assembling technology. They examined chips with 20 μm pitch Cu-SnAg microbumps with bump height $\sim 6 \mu\text{m}$ (3 μm thick Cu and 3 μm thick SnAg). The chips were self-assembled face up on a carrier wafer. Then, the chips were transferred to the corresponding target wafer with microbump-to-microbump bonding through a NCF. The strength of temporary bonding was lower than the microbump bonding through the NCF, and thereby, the chips were removed from the carrier wafer and successfully transferred to the target wafer. After that, the target wafer having the chips bonded upside down on the wafer was packaged by a compression molding technique with a granular resin that covered the self-assembled chips to planarize the chip-on-wafer structure. Finally, the chips and the resin were simultaneously thinned from the backside of the chips. ◀



Dr. Phil Garrou,
Contributing Editor

Wafer bonding enables better LEDs

In my discussions with LED manufacturers in different regions of the world, I have found that engineers are confronting similar challenges concerning wafer bonding, particularly in the processing of vertical LED (VLED) chips. VLEDs offer certain key advantages over their lateral LED counterparts, though the lateral approach is a simpler process.

Both LED designs begin with the epitaxial growth of GaN on a sapphire substrate. However, all subsequent processes differ. In a lateral LED design, the sapphire remains a part of the GaN LED stack. Since sapphire is a perfect insulator, both contacts to the LED diode structure must be formed at the topside of the LED die.

As a result, valuable device real estate is consumed by the electrical connections. Doing a simple back-of-the-envelope calculation of surface loss for a 4-inch LED wafer, assuming 300x300- μm die and 100x100- μm wire-bonding pads reveals that each diode contact, to p-doped and n-doped GaN, consumes about 10 percent of the wafer surface, which is quite significant.

In contrast, with VLEDs, GaN epitaxy is followed by full-wafer deposition of a metal-film stack followed by wafer bonding with a carrier substrate. Since one electrical contact is the bonding layer itself and hence buried inside the LED stack, manufacturers of VLEDs immediately save the aforementioned 10% of real estate. In addition, electrical injection is more efficient for VLEDs, where their lateral relatives have difficulties, especially when current density is increased.

LEDs

However, optimizing the real estate and the electrical efficiency is only one aspect of the process: getting the light

output from the LED remains the challenge. In GaN-based LEDs, the crystal planes of the GaN lead to a concentrated light emission normal to the sapphire's c-plane, i.e., normal to the LED surface. In lateral LED designs, photons also couple into the transparent sapphire wafer so that light is also emitted from the LED's sidewalls. Since losses are higher, efficiency is decreased.

To increase light output in VLEDs, a metallic mirror is deposited prior to the metal bonding layers, leading to the redirection of emitted light to the LED surface. Optimization of light extraction is further enabled by creating a resonant cavity in combination with surface roughening. In addition to improved light extraction efficiency, the light is well directed.

From a material standpoint, many eutectic metal systems (e.g. Au:Sn) or diffusion solders (e.g. Au:In) fulfill these requirements. However, each presents different processing requirements. The chosen metal system determines the bonding temperature. Because the sapphire substrate and the carrier substrates have quite different coefficients of thermal expansion, a metal system with low bonding temperature will keep strain at a more manageable level. The selection of these layers is beyond the scope of this article, but typically metal layers such as platinum, aluminium and gold and combinations of these materials are used.

Next, adhesion and diffusion barriers have to be chosen to contain the diffusive metals from the injection contacts or mirror layer of the LED structure. The correct choices will result in a high-yield layer transfer process.

The potential use of GaN-on-silicon in LED manufacturing is an exciting prospect that seems likely to come to fruition in the next several years. Companies are 2-3 years from entering mass production, with laboratory LED efficiencies comparable to LEDs on sapphire. With a silicon substrate, wafer bonding provides one of the enabling steps of transferring the LEDs after growth.

Note: Originally published in LEDs Magazine. ◀



Thomas Uhrmann,
Business
Development
Manager, EV Group
(EVG).



HIGH VOLTAGE DRIVERS

BCDMOS designed for 700V driver chips

JAE SONG, Dongbu HiTek, Seoul Korea

A specialized ultra high voltage BCDMOS process at the 0.35 μ m node deploys thin n-epitaxial technology to support high voltage applications.

BCDMOS today ranks as a preferred process for implementing system-on-chip solutions, thanks to its capabilities to integrate Bipolar (analog), CMOS (logic) and DMOS (power) functions on a single chip. Within the past few years, the rapidly growing demand for monolithic

while maintaining high breakdown voltage.

Two types of DR-LDMOS structures have been optimized using thin n-epi technology. One is for a switching transistor to increase on-breakdown voltage, and the other is for a level shifter between low and high side regions. Let us now take a closer look at these

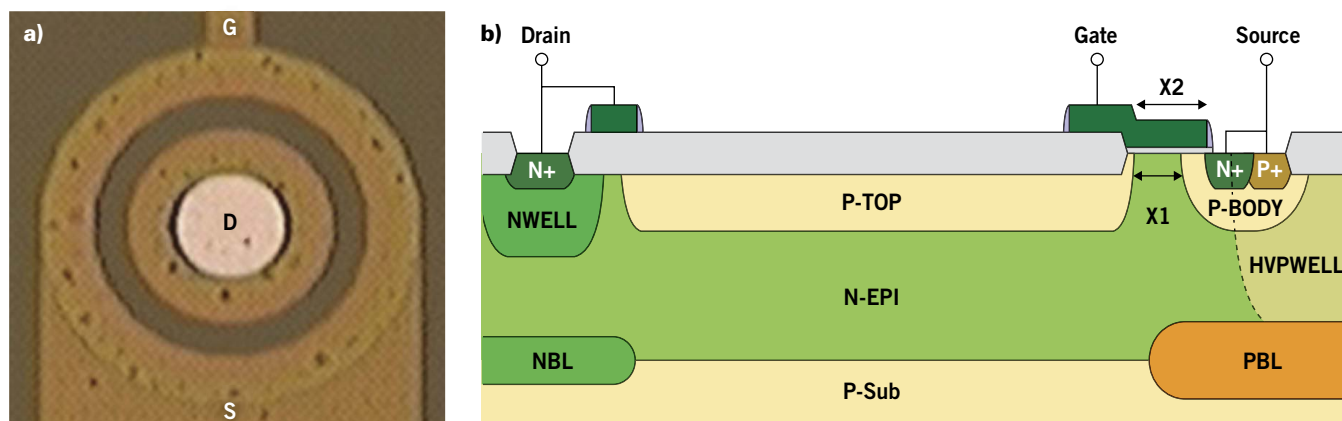


FIGURE 1. Actual DR-LDMOS top view (a) and cross section of 700V DR-LDMOS (b) for level shifter.

smart power ICs has greatly accelerated the evolution of BCDMOS process technologies to support ultra high voltage applications.

Specialty semiconductor foundries have taken leadership roles in expanding the capabilities of BCDMOS to better implement ultra high voltage chip solutions. One of the most promising developments centers on optimizing DR-LDMOS (Double RESURF LDMOS) transistors by using thin n-epi technology and introducing a P-TOP layer to reduce on-resistance

two types to better understand how their structures take BCDMOS process technology to a new level in supporting ultra high-voltage industrial applications.

DR-LDMOS for level shifting

Fig. 1 illustrates an actual DR-LDMOS top view (with circular shape) along with a cross section of a 700V DR-LDMOS structure that forms a level shifter on the high side of the gate driver IC. Significantly, the high on-breakdown voltage transfers a low voltage

JAE SONG is executive vice president of marketing at Dongbu HiTek, Seoul Korea.

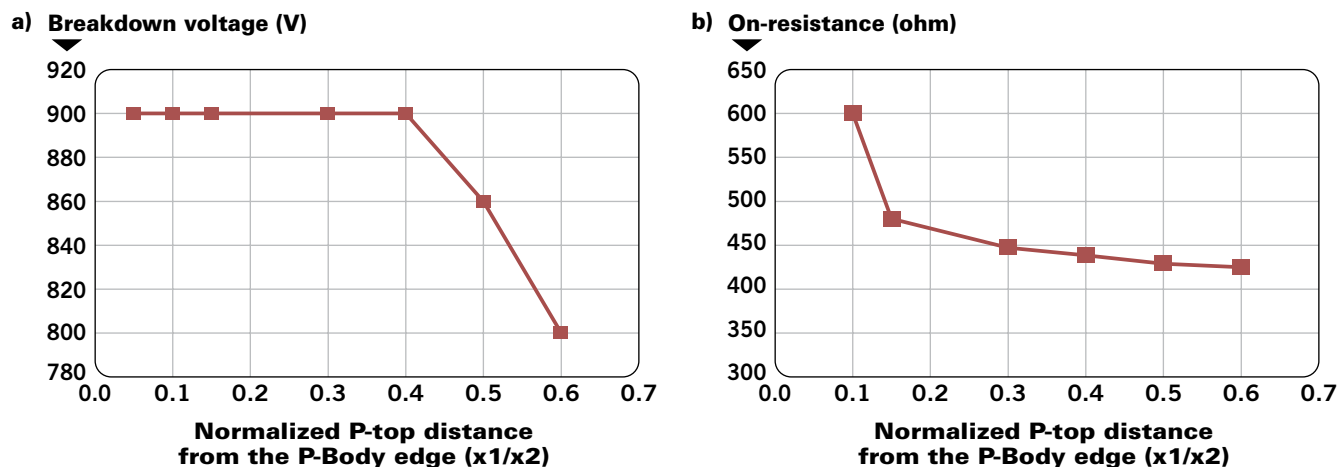


FIGURE 2. Breakdown voltage (a) and on-resistance (b) with variation of P-TOP distance from P-BODY edge.

logic signal to a high voltage control part. Resistance is applied to the vertical JFET between P-BODY and P-TOP in DR-LDMOS to improve on-breakdown voltage as shown in **Fig. 1b**.

Fig. 2 shows the variations of breakdown voltage and on-resistance with the variation of P-TOP distance from the P-BODY edge. As the P-TOP length (X_1) decreases towards P-BODY edge, the on-resistance is increased due to the reduced conductivity caused by increases in JFET resistance. The breakdown voltage increases with the decrease of X_1 due to maintaining an optimal charge balance between n-epi and P-TOP for Double RESURF.

If the X_1 is increased more than 0.4 (X_1/X_2), the breakdown voltage drops drastically from its plateau

voltage due to the high surface electric field under the gate electrode. As a result of optimizing JFET resistance for DR-LDMOS, an on-breakdown exceeding 700V is achievable at the optimal condition ($X_1/X_2=0.4$) and the off-breakdown voltage exceeds 900V as shown in **Fig. 3**.

DR-LDMOS for switching

Fig. 4 shows a cross section and layout schematic of DR-LDMOS transistor with multi fingers for switching applications. This device is applied to a Double RESURF structure with an additional PTOP layer inside and an extended n-type drift region (n-epi) to reduce on-resistance.

The DR-LDMOS consists of the regions shown in

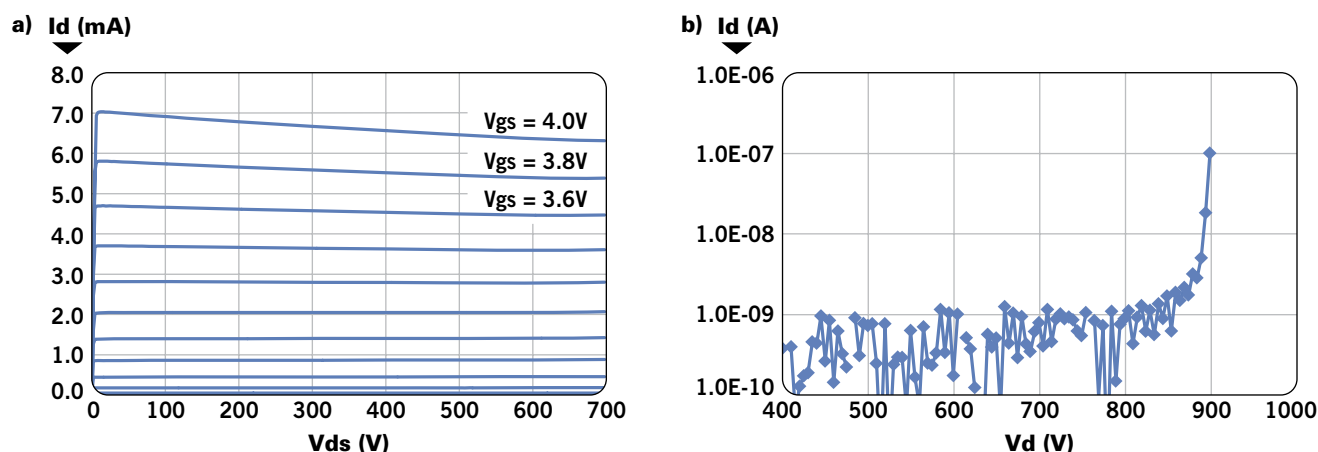


FIGURE 3. DR-LDMOS I-V characteristics for level shifter (a) and breakdown voltage (b).

HIGH VOLTAGE DRIVERS

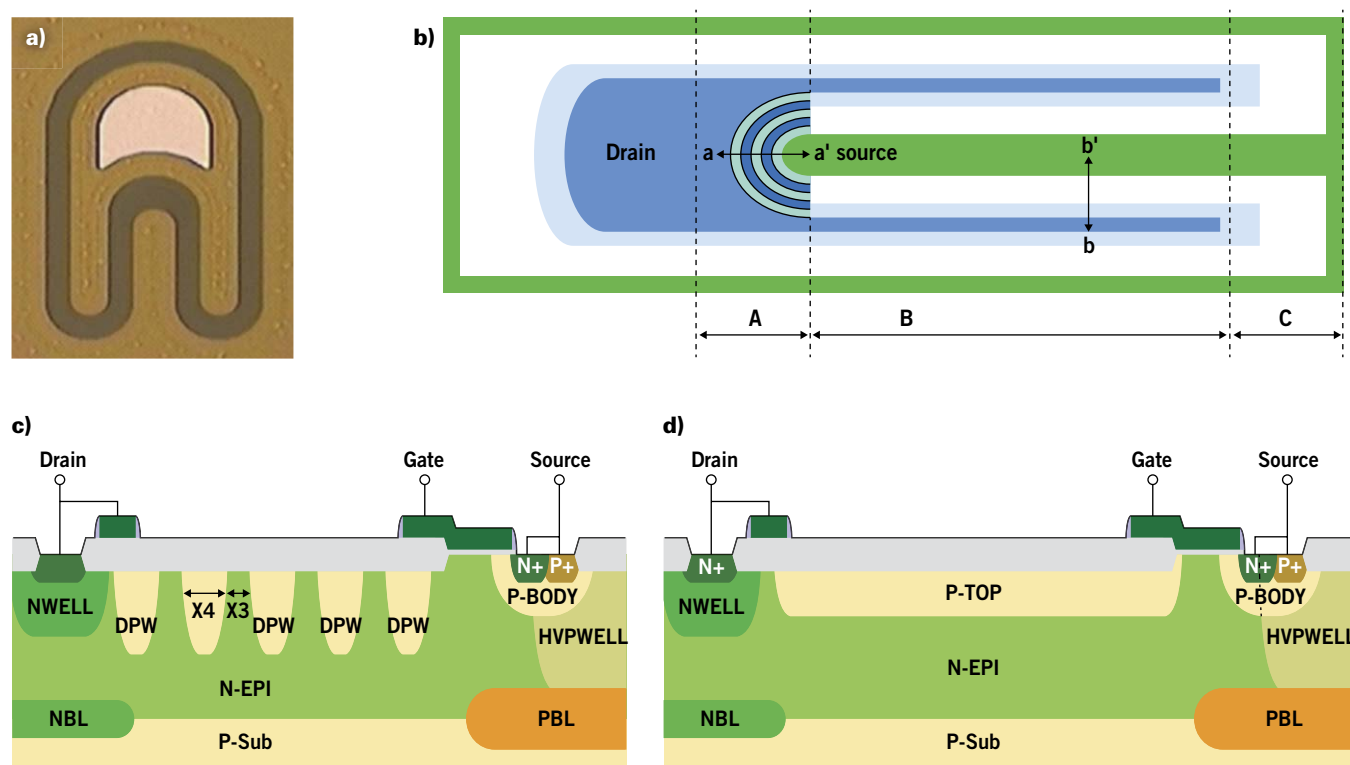


FIGURE 4. Layout schematic and vertical structure of the LDMOS for switching applications. Actual DR-LDMOS top view (a); general LDMOS layout (b); cross section of source corner region a-a' (c); cross section of stripe region b-b' (d).

Fig 4. Stripe region (B) and drain corner region (C) maintain high breakdown voltage due to optimal charge balance between n-epi and P-TOP layer. However, source corner region (A) breakdown voltage is decreased dramatically due to the high surface electric field under the gate electrode caused by a broken charge balance between n-epi and P-TOP. To overcome this problem, the DR-LDMOS deploys an HVPWELL

layer with rainbow shape at the source corner region as shown in **Fig. 4c**.

As the distance X3 between HVPWELL decreases, the breakdown voltage increases due to the reduction of the high surface electric field under the gate caused by a decrease of n-type charge regarding dilution of n-epi concentration. As shown in **Fig. 5**, the optimal

Continued on page 23

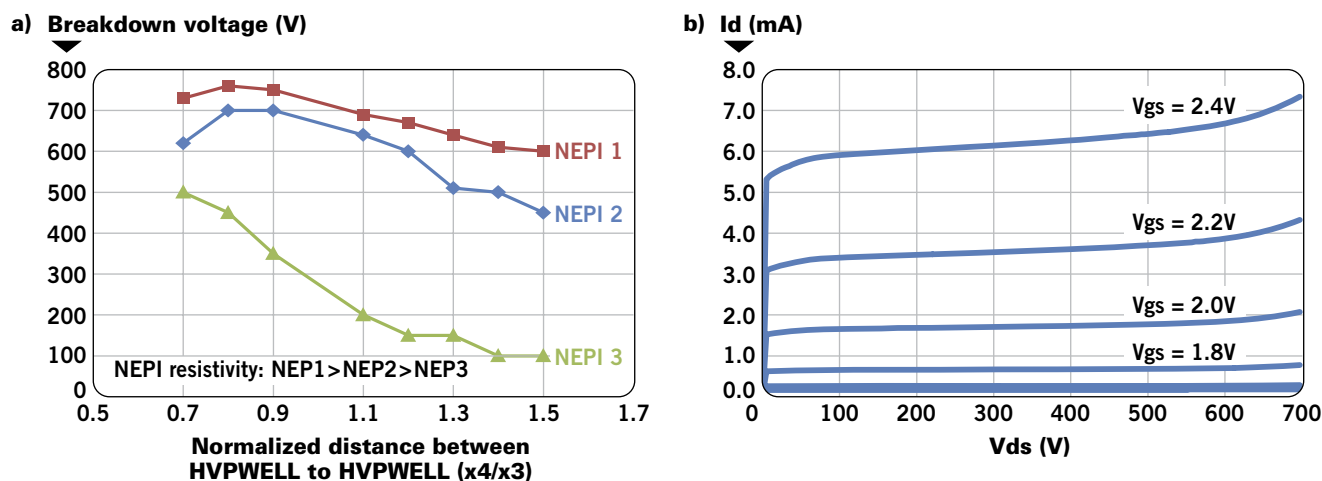


FIGURE 5. Breakdown voltage with the variation of distance between HVPWELL (a) and measured I-V with optimal condition ($X_4/X_3=0.8$) of NEPI 1.

DISPLAYS

Material support: helping displays deliver higher performance

ANDREAS WEISHEIT Linde, Shanghai, China, and **GREG SHUTTLEWORTH**, Linde, Guildford, UK

Metal oxide transistors increase electron mobility by a factor of up to 40 compared to conventional technology, at a comparable cost base.

With the rapid development of advanced display technologies, such as OLED, high definition 3D and smart displays, continuing to deliver improved performance is challenging traditional display manufacturing techniques. New materials and manufacturing approaches will be required to deliver display products with the features and functionality demanded by customers but at market friendly prices and with a reduced environmental impact.

Conventional TFT-LCD display manufacturing is a

focus on the thin-film transistor process (**Fig. 1**).

Transistors control the pixels and switch them on and off. The type of transistors and the processes used for their manufacturing determine the performance of the display, the costs, and, to a large extent, the environmental footprint of the device. Today, two transistor types are common in mass production; amorphous silicon (a-Si) transistors are dominant (>95%), while low temperature polysilicon transistors (LTPS) have a niche position.

The manufacture of Ultra High Definition (UHD) 3D

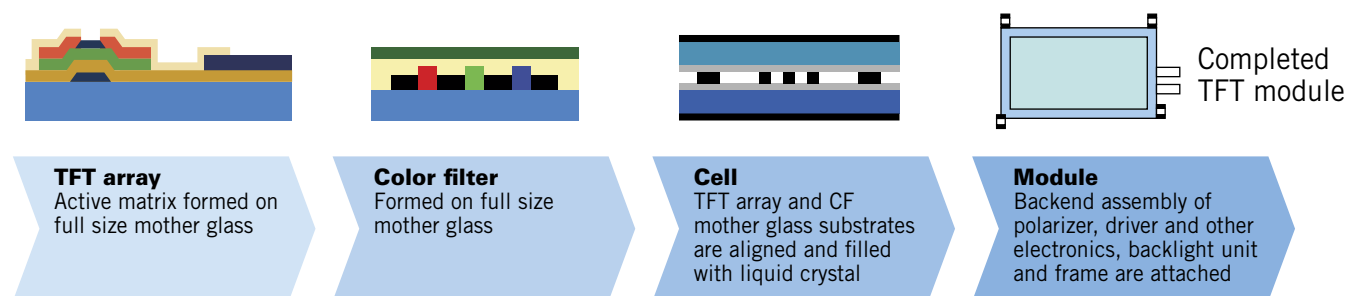


FIGURE 1. TFT-LCD display manufacture is a sequence of complex processes, which can be classified in the four categories shown.

sequence of complex processes, which can be classified in 4 categories: first forming of an array of thin-film transistors (TFTs) on the mother glass, second forming of a color filter, followed by the cell process where substrates are filled with liquid crystals, and finally the back-end assembly of the module. From a semiconductor and electronics materials perspective, we will

displays (3840 x 2160 pixels) is currently not possible using conventional amorphous silicon transistors, because when these are scaled down in size (in order to keep the pixel size small) they don't conduct electrons quickly enough to maintain the fast frame rates required. Improving electron mobility in transistors is crucial in bringing higher resolutions and higher frame

ANDREAS WEISHEIT is the Head of Global FPD and Asia Market Development at Linde and **GREG SHUTTLEWORTH** is an equipment product manager at Linde.

DISPLAYS

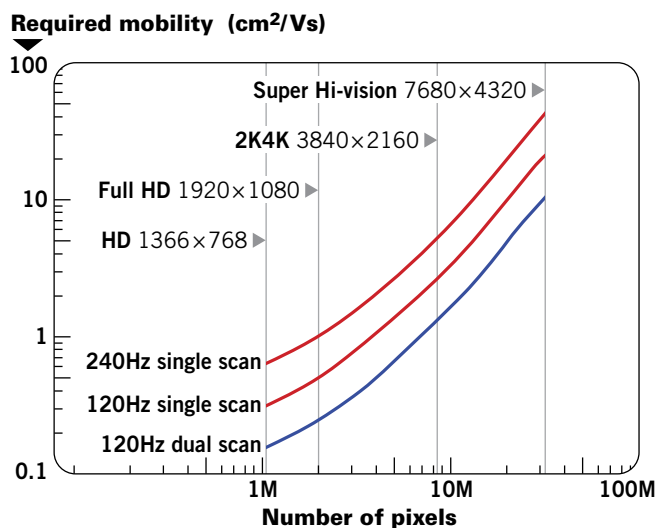


FIGURE 2. Summary of electron mobility required for future displays. [1]

rates to TVs, mobile and computing devices (**Fig. 2**). Polysilicon transistors could deliver the required performance but would cost up to twice as much as the manufacturing process becomes more complex. A more promising approach is to use metal oxide transistors. This will increase electron mobility by a factor of up to 40 compared to conventional technology, at a comparable cost base as the process flow remains similar.

Enabling UHD 3D is only one of the benefits of smaller transistors. They also allow more light to pass from the backlight through the backplane, reduce power consumption and increase battery life of mobile devices. Moreover, they also allow the higher currents needed to drive OLEDs. Consequently, the majority of leading display manufacturers have recently announced plans to launch products with metal oxide transistors. Samsung introduced a 55-inch OLED TV at the 2012 Samsung Premium TV Showcase in May of this year, and LG Display unveiled plans to launch a 55-inch OLED TV by the middle of 2012. Additionally, Sharp has announced that the company has started the commercial production of metal oxide displays in its Kameyama plant.

Metal oxide transistors

The channel of metal oxide transistors is mostly made from IGZO (indium, gallium and zinc oxides). The gate dielectric isolates the gate from source and drain. The passivation layer seals and protects the transistor (**Fig. 3**).

The formation of gate, dielectric, source drain and passivation layers is carried out through a sequence of deposition and etching steps to create the required patterns. This is where specialist gases and materials play a key role. The metallic layers (gate, channel and pixel layers) are typically deposited using physical vapour deposition (PVD). Here, argon atoms strike a solid target and sputter the material on to the substrate. Plasma enhanced chemical vapour deposition (PECVD) is used for the deposition of dielectric and passivation films. PECVD uses large amounts of silane (SiH_4) as a silicon precursor and ammonia (NH_3) as reactant to form silicon nitride (Si_3N_4). Hydrogen and nitrogen are used as carrier gases, while phosphine (PH_3) is used for doping films. Etching of films is typically carried out using fluorinated gases which react with the films to create volatile compounds which can then be pumped away.

Since metal oxide channels are used to enable very high performance, changes in the dielectric and the passivation will be required as well. Both functional layers will change to silicon oxide (SiO_2) which offers better stability and moisture protection than silicon nitride. To enable this change at production volumes, the PECVD process will require high volumes of high-purity nitrous oxide (N_2O) as reactant rather than ammonia (NH_3). While we are familiar with the use of this gas in dentistry, the volumes and purity required for displays present new challenges for the materials industry. The shift from silicon to metal oxide transistors would not be possible without a secure supply of high-purity N_2O , which highlights the critical role that specialty gases and materials play in enabling the development of next-generation consumer electronic devices.

Deposition processes also deposits quantities of material on the inside of the process chamber, which must be periodically cleaned to maintain process cleanliness and production efficiency. Both these cleaning processes and etching steps described earlier use fluorine based gases, and given that process chambers need to accommodate glass substrates with an area of more than five square metres, the amount of gas required is very large.

Why is this important? The gases traditionally used have very high global warming potential (GWP). Sulphur hexafluoride (SF_6) used for etching, has a GWP

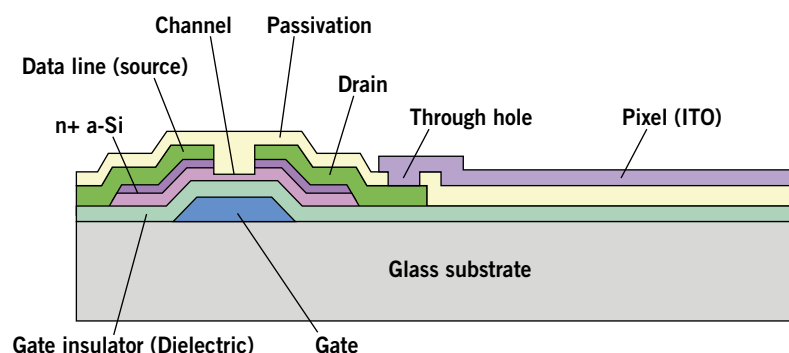


FIGURE 3. Cross-sectional view of a metal oxide thin film transistor used in displays.

23,900 times that of CO_2 , while nitrogen trifluoride (NF_3) used for cleaning, has a GWP of 17,200. So with a typical Gen 8 facility using upwards of 300 tons of such gases per year, the potential environmental impact must be considered.

The case for F_2

To minimize process emissions, most manufacturers have installed high performance scrubbing systems. However, there exists the risk of emissions during the whole life cycle of the material. Measurements by the Scripps Institute [2] have shown a rapid growth in the amount of NF_3 present in the atmosphere, which correlates to a figure as high as 16% of NF_3 produced ultimately escaping. There remains an incentive to consider materials with lower GWP to minimise the impact of emissions due to the manufacturing, transport and disposal of the materials, areas outside the control of TFT-LCD manufacturers. One strong contender is fluorine gas (F_2).

The science goes like this. NF_3 or SF_6 gas is activated by a plasma to release fluorine radicals which then etch or clean the silicon films. The alternative, F_2 gas, is the simplest molecule containing fluorine atoms and has the lowest bond energy. These properties of F_2 provide significant benefits to the cleaning and etching processes; faster etching or cleaning, less tool down-time, reduced gas use, and less electrical power consumed by the plasma to break down the simpler F_2 molecules.

Chamber cleaning using F_2 rather than NF_3 has been used in TFT-LCD production for some years now, delivering reductions in mass of gas required of 20%

along with improved tool productivity due to a 30% reduction in cleaning time and almost 50% reduction in plasma power consumption. More recently, fluorine was evaluated as a direct replacement for SF_6 for the etching process. Evaluation results on a Gen 4.5 size panel showed significant improvements in etch rate and etch uniformity when using fluorine for both silicon oxide and nitride films while maintaining the same feature taper angle.

Environmentally speaking, the big win is the zero GWP of F_2 . To highlight the impact, **Table 1** shows the potential CO_2 equivalent savings from replacing NF_3 with F_2 in a typical large scale TFT-LCD fab chamber-cleaning process.

It is thus likely that the replacement of NF_3 and SF_6 in the display manufacturing process can have a larger overall environmental benefit for TFT-LCD manufacturers than is achievable by any other means.

Conclusion

While you enjoy the stunning resolution and performance of the latest displays and reflect on the reduc-

TABLE 1: Potential CO_2 equivalent savings from replacing NF_3 with F_2

		Typical Gen8 fab
NF ₃ consumption per year (tons)		>300
CO ₂ eq emissions (tons) = 300 x 17,200 x 16% (ref 2 Scripps data)		>825,600
CO ₂ eq emissions (tons) = 300 x 17,200 x 10% (conservative figure)		>516,000

tions in power consumption and increases in battery life, the materials industry will have played a key supporting role, from developing new materials for device research and development to delivering the materials at the quantities and purities required for pilot and mass production and for continuous improvement of the more established processes for better efficiency, lower costs and reduced environmental impact. ◀

References

1. T. Kamiya et al., "Present status of amorphous In-Ga-Zn-O thin film transistors," *Science and Technology of Advanced Materials*, 11 (2010)
2. R. F. Weiss et al., "Nitrogen trifluoride in the global atmosphere," *Geophysical Research Letters*, vol. 35, October 2008

TEST

Testing probe cards that contain complex circuitry

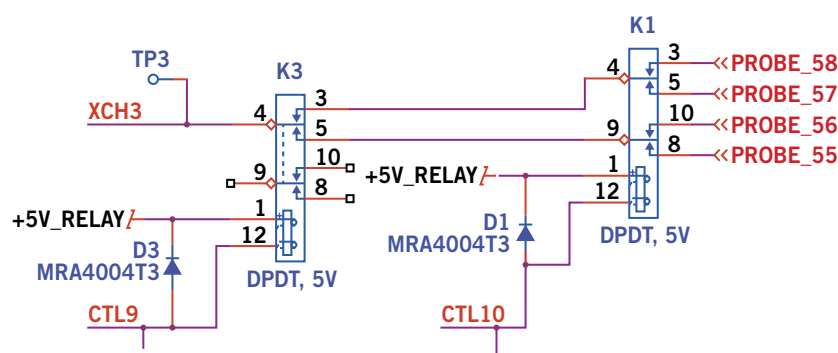
GREG OLMSTEAD and BOB DAVIS, Rudolph Technologies, Inc., Flanders, NJ

State based testing is a simple, highly scalable method to describe activation details for probe card circuitry.

As the complexity and cost of integrated circuits and packaging technologies continue to increase, so also does the need for more sophisticated testing capability. This has resulted in the development of highly advanced probe cards, which provide the mechanical and electrical interface between the tester and the integrated circuit. In addition to tremendous increases in the number of probes and channels, probe density, and probing forces, current generation probe cards also incorporate complex circuitry to support advanced functionality. Both manufacturers and users of probe cards use probe card analyzers (PCA) to monitor and maintain probe cards and ensure the integrity of the testing process. At the most basic level probe card analyzers measure the mechanical position and electrical continuity of the probes. However, on today's more advanced probe cards, the PCA must also monitor the functionality and performance of on-card circuitry and components.

Evolution of probe card complexity

The first test probes provided no more than a direct



CTL10	CTL9	Connection	State name
Open	Open	XCH3..Probe58	STATE_P58
Return	Open	XCH3..Probe57	STATE_P57
Open	Return	XCH3..Probe56	STATE_P56
Return	Return	XCH3..Probe55	STATE_P55

Channel label	State label	Probe label	Primary channel res (Ohms)	Primary channel
XCH3	STATE_P55	Probe55	8.257	Passed
XCH3	STATE_P56	Probe56	8.922	Passed
XCH3	STATE_P57	Probe57	14.061	Passed
XCH3	STATE_P58	Probe58	9.608	Passed

FIGURE 1. Relay switching can increase the number of connections permitted for a limited number of test channels. Here a pair of relays connects a single channel to any one of four probes (top). State definitions specify activation conditions for two control lines (middle). Results reference the state label for each measurement (bottom).

conductive mechanical/electrical contact to a test pad or exposed node of the integrated circuit. Multiple probes were soon arranged on a probe card to provide

GREG OLMSTEAD is Senior Member of Technical Staff and BOB DAVIS is Staff Software Engineer at Rudolph Technologies, Inc., Flanders, NJ.

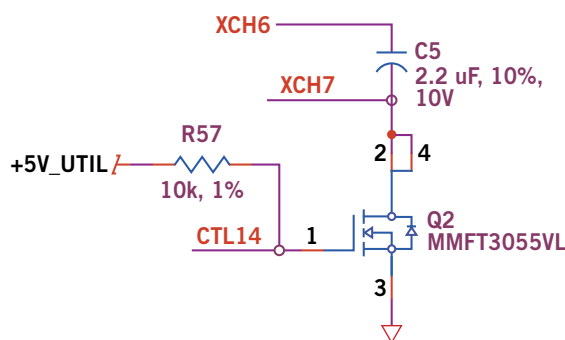
multiple simultaneous contacts. Probe card analysis in these early cards focused simply on measuring the positions (X,Y and Z) and electrical properties (contact resistance, leakage current, capacitance) of the probe tips.

The circuitry on probe cards evolved rapidly, beginning with the addition of passive components such as capacitors and resistors, and quickly expanding to include relays and other active circuitry designed to extend the I/O resources of a given tester platform. The PCA then had to supply power and control to the relays and verify the switched pathways.

Advanced probe cards now often incorporate local power management, digitally controlled analog switching, probe card heating, and non-volatile storage for identification and touchdown history. They may also include devices such as opto-couplers, voltage regulators, PLDs, FPGAs and microcontrollers. Circuits can use latched or sequenced inputs, and serial or other communication protocols to control states and potentially provide feedback on the health or state of the “on board” control circuits.

State-based testing

These on board circuits constitute, in effect, an electrical barrier between the tester side of the probe card and the probe tips. They must be manipulated and controlled in order to measure probe characteristics. The circuitry included in many current probe card designs has reached a level of complexity that makes it impractical to control individual components manually. State based testing is a strategy to simplify circuit testing by collecting all of the required activation conditions into a single “state” definition. Simply recalling a predefined state allows the PCA to do what is necessary to activate the circuit while the user gets on with testing the probe card. The state definition may be a static definition of an array of I/O conditions or may include sequences of conditions that must be executed in order to bring the circuit to the desired state.



From: Channel label	To: Channel label	State label	Expected capacitance (uF)	Measured capacitance (uF)
XCH6	XCH7	(any)	2.2	2.153
XCH6	GND	ST_Q2_OFF	0.001	0.001
XCH6	GND	ST_Q2_ON	2.2	2.154

FIGURE 2. Good design-for-test practice provides connections for component testing as well as probe switching. In this example XCH7 is connected to a node between the capacitor and the FET switch, permitting direct, isolated testing of each component.

Design-for-test

In addition to being able to manipulate the probe card components to enable measurements of probe characteristics, the PCA must be able to test the performance and functionality of the individual components themselves. This requires probe card manufacturers to design-for-test, being sure to provide access to all of the various control elements and signal nodes needed to enable thorough and complete test procedures.

For each probe card circuit, card designers and test engineers must define the required challenge and response, decompose the circuit function, identify a means of circuit activation in the probe card analyzer, and specify control conditions sufficient to achieve activation. With state based testing, the use of predefined activation states greatly simplifies the task of establishing the activation conditions required to make the desired measurements.

Relay switching

Relay switching is a way to increase the number of connections available to a limited number of test channels. Consider a simple multiplexer composed of a pair of double pole, double throw relays configured to switch a single channel among four connections. The

TEST

connection is determined by the states of the two relays (**Fig. 1**). Defining a state name for each of the four possible combinations of relay states permits simple measurement of the resistance for each connection.

Simple switching for component validation

In **Fig. 2**, an FET switch controls a bypass capacitor. There are no probes in this example. It is provided to illustrate the importance of exposing nodes to enable component verification. When CTL14 is at logic 1, FET Q2 is closed. When CTL14 is at logic 0, FET Q2 is open. Capacitor C5 is removed from the circuit by default, but is connected when FET Q2 is on (State = ST_Q2_ON). XCH7, connected between the switch and the capacitor, allows direct and isolated measurement of C5, and direct and isolated measurement of Q2 drain-source resistance in both on and off states.

Analog IC switching

Analog switching can be much faster, consumes less power and allows greater density than relay based switching. It permits much greater flexibility in

configuration but can present challenges to probe card analysis, such as large numbers of connections or the sharing of control returns with other “grounds”. It has the potential to be configured via on-board logic without much “driver overhead”, further increasing its flexibility but creating combinations of challenges for probe card analysis.

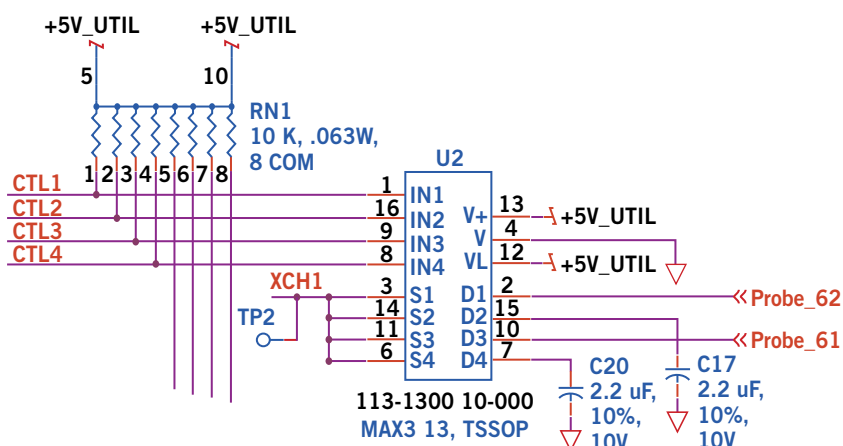
In the example shown in **Fig. 3**, the IC is a quad single pole single throw analog switch connecting XCH1 to any of Probe 61, Probe 62, C17 or C20. CTRL lines 1-4 select the address of these options. Pull up resistors make the hardware default ON. In the State Labels the default condition for all switches is open (contrary to the hardware default). In contrast to the combinatorial control scheme illustrated above for the relay switch, here each switch is controlled independently by the condition of a single CTRL line, providing simple mapping and arbitrary flexibility.

Stateful control

Stateful control satisfies the need for more complex control and monitoring of functions such as switching, power health, identification, verification state and more. It scales easily with probe count, channel count, the amount of switching and the amount of control fanout. It simplifies activation of the desired state through the extension of state based control to include time based control sequences. It can also incorporate feedback from the device under test to the probe card analyzer.

Another important benefit of state based testing is its ability to support thorough and complete testing without exposing details of the circuit design, allowing probe card manufacturers to encapsulate and protect their intellectual property.

The schematic shown in **Fig. 4** illustrates the large number of connections and complexity typical of current probe card designs. As shown in the block diagram, the circuit switches 24 I/O lines among 4 identical 24-probe site



Channel label	Expected resistance (Ω)	Measured resistor (Ω)	Probe label	State label
XCH1	Open	>40M	PROBE_61	DEFAULT
XCH1	15	22.293	PROBE_61	Probe61
XCH1	Open	>40M	PROBE_62	DEFAULT
XCH1	15	22.641	PROBE_62	Probe62

FIGURE 3. Analog IC switching can be much faster, consumes less power and allows greater density than relay based switching. In this example each switch is controlled independently by the condition of a single CTRL line, providing simple mapping and arbitrary flexibility. State based testing scales readily to the larger number of connections typical of analog IC designs.

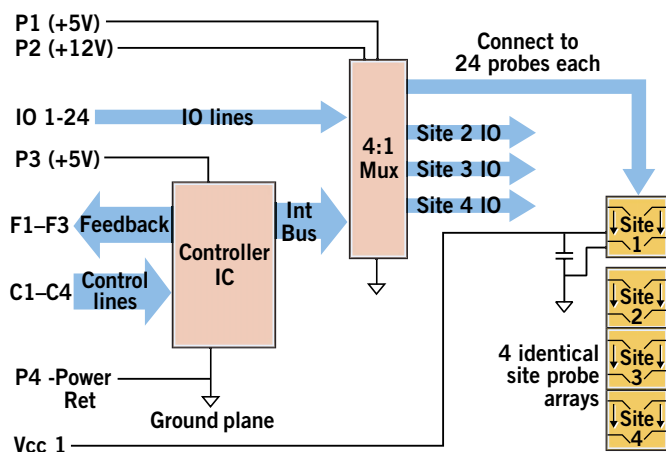


FIGURE 4. Current generation probe cards may incorporate very complex circuitry with digitally controlled sequential logic. State based testing scales easily with size and complexity and readily accommodates activation sequences and feedback from the card. This circuit multiplexes 24 I/O lines among 4 separate 24-probe site arrays.

arrays. Control and feedback lines operating through a controller IC provide information on the health and status of the circuit. Control lines may be more numerous and may include sequential control schemes.

Conclusion

The complexity and cost of probe cards used to test integrated circuits have increased dramatically, making probe card analysis both more challenging and more valuable. State based testing is a simple, highly scalable method to describe activation details for probe card circuitry to enable traditional probe card testing as well as thorough and complete testing of on board circuitry. Combined with PCA-aware design-for-test, state based testing can maximize PCA verification of probe cards with increasingly complex circuits, while simplifying the process. State based testing also provides important protection for intellectual property by supporting testing without exposing details of the circuit design. ◀

HIGH VOLTAGE DRIVERS

Continued from page 16

distance (X_4/X_3) is between 0.7 and 0.9, and the breakdown voltage is over 750V at the NEPI1 condition.

Conclusion

Two types of robust 700V DR-LDMOS transistors using thin epitaxial technology have been developed for level shifting and switching applications. The P-TOP layer is introduced to reduce on-resistance while maintaining high breakdown voltage for a switching transistor, while also increasing on-breakdown voltage for level shifting between low and high side regions. By optimizing JFET resistance of DR-LDMOS for level shifting, the on-breakdown can exceed 700V at the optimal condition ($X_1/X_2=0.4$) and off-breakdown voltage can exceed 900V. For switching applications,

an HVPWELL layer of rainbow shape is deployed at the source corner region to reduce n-type charge of the n-epi region and achieve a breakdown voltage that exceeds 750V. ▶

References

1. J. Appels, H. Vaes & J. Verhoeven, High voltage thin layer devices (RESURF Devices)," *EDM. Tech.Dig.*, 1979, pp.238-241
2. J. Appels, M. Collet, P. Hart, H. Vaes & J. Verhoeven, "Thin layer high voltage devices (RESURF devices)," *Philips Journal Research*, vol.35, 1980, pp.1-3
3. Zia Hossain, "Determination of Manufacturing Resurf Process Window for a Robust 700V Double Resurf LDMOS Transistor," *Proc of ISPSD*, 2008.
4. Nam-Chil Moon, Bon-Keun Jun, Kyoung-Wook Kwon, et al, "Design Optimization of two kinds of robust 700V DR-LDMOS using a thin epitaxial layer," *PCIM presentation* (Nuremburg, Germany) May 8, 2012

PACKAGING

Defect detection in die stacks with acoustic imaging

TOM ADAMS, Sonoscan, Inc., Elk Grove Village, IL

A new simulation technique makes imaging easier and faster for stacked die and other multi-layered structures.

Manufacturers of stacked die configurations have a strong interest in learning by non-destructive means whether a device contains defects such as delaminations, and exactly where the defects are. The standard method for nondestructive imaging and analysis of internal structural defects in other component types has long been acoustic microscopy, but stacked die have always presented a problem because their multi-layer structure makes accurate acoustic analysis difficult. After years of work in collaboration with the Technical University of Dresden, Sonoscan has recently unveiled a simulation technique that makes imaging easier and faster for stacked die and other multi-layered structures.

Challenges for imaging stacked die

Acoustic microscopes use a scanning transducer that switches thousands of times a second between pulsing ultrasound into a sample and receiving the return echoes. This is known as reflection-mode acoustic imaging. The general behavior of ultrasound when pulsed into a sample is straightforward: when the focused beam strikes the interface between two dissimilar materials, it is partly reflected and the remainder is transmitted deeper into the sample. However, it is virtually 100% reflected at an interface between a solid material and the air in a delamination, crack, void or other gap. In the case of an air gap interface there is no further ultrasound transmission

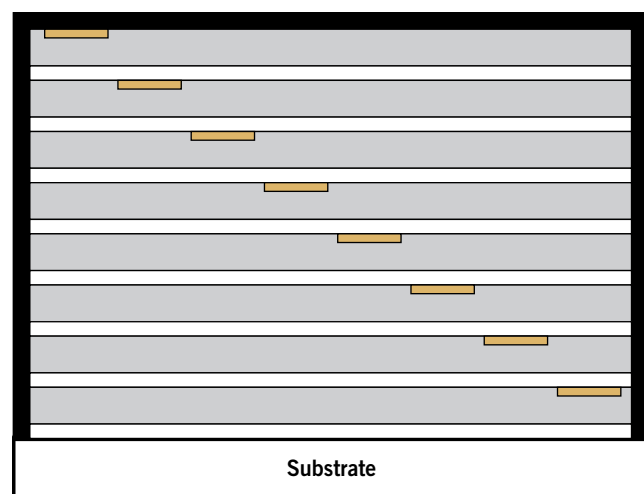


FIGURE 1. Diagrammatic side view of a typical die stack, showing the numerous material interfaces. Test stacks generally have gaps (gold in diagram) etched into the top of each die.

deeper into the sample thereby blocking reflection mode views of deeper structures.

Ultrasound behaves in this way in all of the many electronic components that are imaged acoustically. What makes stacked die dramatically different is that there are many layers causing reflections and if the layers are equal thickness, as in many devices such as memory chips, the echoes can overlap making it difficult to distinguish the individual layers. In addition, since the signals from deeper layers are weaker than those from the top layers due to reflection losses at each subsequent interface it may be harder to identify the relevant echo.

TOM ADAMS is a consultant with Sonoscan, Inc., 2149 E. Pratt Blvd., Elk Grove Village IL USA 60007, Phone: 847 437-6400, E-mail: info@sonoscan.com, website: www.sonoscan.com

Creating the simulated die stack

In order to help image individual layers of a stacked die sample the simulator tool uses construction information from the sample to predict the echo patterns that will result from using a pre characterized transducer in the C SAM acoustic microscope. In the block diagram below, the operator places virtual defects at any or every layer of interest and then the program calculates the echo patterns for each condition. The construction data includes thicknesses and properties of each layer. If exact properties are not known there may be some error in the result, however, the program will still give the analyst enough information to make the imaging task more efficient.

An engineer who needs to inspect the die in a stack for gap-type defects can use the simulation module, which has two main functions:

- It allows the engineer to create a simulated die stack that is as similar as possible to the physical die stack that he needs to image.
- It allows the engineer to acoustically image the simulated die stack that he has created.

To create the simulated die stack, he needs to know the part construction of the physical die stack: the material characteristics and the precise thickness of the various layers, for example.

By entering these values into the simulation software he creates the virtual die stack. **Figure 1** is the diagrammatic side view of a die stack, showing the individual die and die attach layers. In making the virtual die stack using the simulator, the operator will enter values that create highly reflective simulated defects, typically one defect at each interface. The simulated defects are shown in gold in the diagram. In the simulation, these gaps will reflect ultrasound just as real defects do. They are typically staggered from left to right to avoid overlap and to identify the individual layers.

When the simulated die stack is complete, the engineer will select the ultrasonic transducer that best images this particular sample.

He will gate the A-scan echoes (echoes from all interfaces below a single x-y position) to isolate the defect that he has placed, for example, on top of die #3 when entering values to create the virtual die stack. Gating is accomplished by moving two vertical

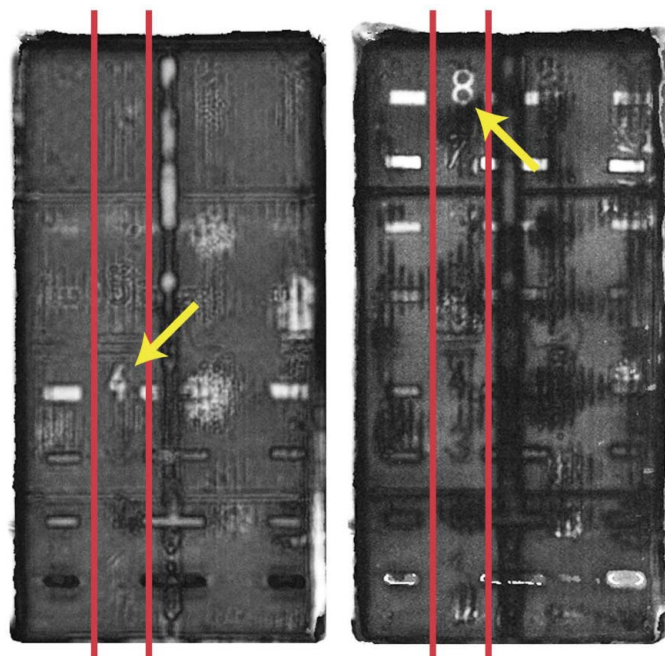


FIGURE 2. Right half of an 8-die test stack, imaged with parameters derived from the simulation, and gated and focused on die #4 and #8 (at the bottom of the stack). Red bars enclose the vertical columns of all eight numerals. Gated and focused numerals are bright; the others are dark or not visible.

bars on the on-screen echo waveform to enclose the precise echo depth that will be encompassed in the acoustic image. Echoes reflected from the gated depth are used to make the image; echoes from other depths are ignored.

Next he will move to the C-scan imaging mode using the simulated data, which uses the virtual transducer to scan the area of interest that includes the defect at die #3. This will produce a visible acoustic image of the simulated defect. Here he can begin to optimize the gate (i.e., adjust the vertical bars) by moving slightly off the defect, noting changes in the waveform and then moving back onto the defect. By repeating this process he can find the depth range that provides the optimal image of the defect that he has simulated.

Imaging the physical die stack

At this point the simulation has, for the moment, done everything it can do. The engineer turns now to the physical die stack and places it on the real stage of the microscope. His parameters — focusing, gating —

PACKAGING

have already been defined by the simulation. and are transferred from the simulation software to the real-world Sonolytics™ software used to operate the acoustic microscope. When he gates on die #3 in the physical sample he may or may not find a defect, but he will be imaging the interface at the top of die #3 where a defect would lie.

He can optimize the gate and the focus to improve the image of the real interface at die #3, gather a VRM (Virtual Rescanning Module) file, and then transfer the VRM file back to the imaging portion of simulation module to apply the powerful imaging techniques available in the module to the real (as opposed to simulated) data in the VRM file. He may find, for example, that the simulator gate was a bit to the right or left, compared to the gate in the physical sample. By moving back forth between the simulation module (to improve gating) and Sonolytics (to improve focus), he will obtain the best possible acoustic image of the features in the real sample. When the optimal image has been obtained, several advanced imaging modes can further enhance the image.

Figure 2 is the acoustic image of die layers #4 and #8 in an eight-die stack whose imaging parameters were defined using the simulation program. Each silicon die is 75mm thick, and the adhesive between

the die is 40 microns thick. These die stacks were made for testing purposes. Each die contains two types of gap-type features:

- An identifying numeral from 1 to 8 etched into top surface of the silicon. This numeral identifies the die. Die 1 is at the top of the stack, and die 8 at the bottom. The interface between the epoxy die attach material and the shallow gap creates a highly reflective interface. As described earlier for the simulated stack, the numbers are staggered left to right to avoid overlap.
- Three etched slots arranged in a line across the width of the die. Like the etched numerals, each group of slots is staggered.

The stack was not encapsulated, but was covered by a 100 micron layer of foil that was attached to the top die by 11 microns of adhesive.

The key identifier for each die is the numeral. When the operator has completed the simulation program and is accurately focused and gated on a given die, the numeral (in the case of this die stack) will appear relatively bright, while the numerals identifying other layers will appear dark.

The two pairs of vertical red bars in Fig. 2 identify the vertical rows of numerals. At left, the test stack is focused and gated on die #4, whose numeral is bright. The other 7 numerals are either darker or not visible. In the image at right, die #8, at the bottom of the stack, is in focus and accurately gated. In a non-test sample, the results of simulated imaging would give parameters that would gate and focus accurately on each die, even though it has no identifying marker.

Figure 3 is a portion of an acoustic image gated and focused on die #2. The numeral 2 is bright, and the numerals 1 and 3 are visible. The numerals on layers 4 and above, however, are not visible.

The method can be used on die stacks both before and after encapsulation, although imaging through encapsulation will limit imaging to lower acoustic frequencies. The chief advantage of the simulation module is that it greatly accelerates the task of finding the optimum gate for imaging a specific depth of interest. It might be possible to find this gate working only with the physical die stack, but the work would be very tedious, not intuitive and very time-consuming. ◀▶

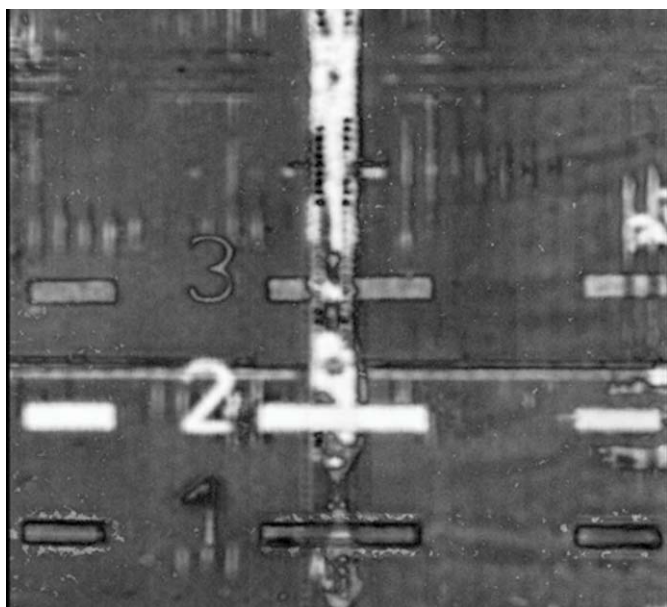


FIGURE 3. Detail of the same test die stack gated and focused on die #2.

LITHOGRAPHY

Understanding shape-dependent mask CD uniformity

AKI FUJIMURA, D2S, Inc., San Jose, CA

Process development teams will need to consider the impact of shape-dependent mask CD uniformity on design rules and wafer yields.

The increasing complexity in mask designs—in particular the growing use of complex sub-resolution assist features (SRAFs) at 20nm-and-below process nodes—has given rise to new mask quality and cost challenges. The proliferation of complex mask features has made shape-dependent mask critical dimension uniformity (CDU) an important new factor that impacts both design rules and wafer yield.

To create complex mask features, OPC groups expend a great deal of effort to compute precisely the desired shapes on the mask. However, the benefits from this effort are partially lost when the shape on the mask has a low tolerance to manufacturing variation. The complex mask features required for leading-edge, critical-layer masks have a shape-dependent mask CDU problem. In this way, we have the undesirable effect that the more precisely the shape is calculated, the less likely that the exact shape will print reliably on the mask. However, if the masks with complex features can be written more reliably, the benefits from these complex mask shapes—even ideal inverse lithography technology (ILT) shapes—will be fully realized, which will make a positive impact on wafer yield and/or design rules.

New mask-manufacturing technologies and techniques have emerged to address these challenges, including model-based mask-data preparation (MB-MDP), mask process correction (MPC), e-beam dose modulation, and the use of overlapping e-beam

shots and circular shots. These techniques have demonstrated, through multiple industry collaborations, an ability to improve shape-dependent CDU. For the first time in many years, a new set of ideas in mask data preparation has emerged to make critical contributions to tightening design rules and improving wafer yield.

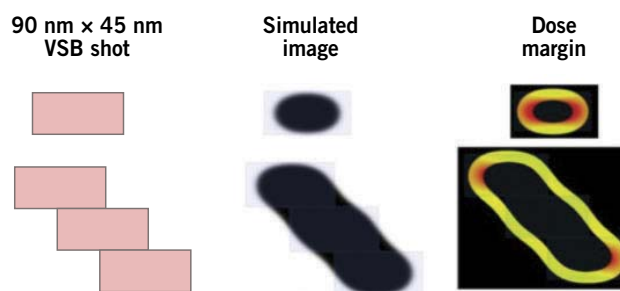


FIGURE 1. The single 90nm x 45nm shot (top) has poor dose margin. The same shot, when repeated and stacked three in a row, has acceptable dose margin. The impact on CDU is shape dependent.

Design rules, wafer CDU and mask CDU

A critical part of any new node is the establishment of design rules. Design rules govern how much functionality can be squeezed into a given area on the wafer, while still having that wafer yield predictably well. There is constant tension between the design-side desire for liberal design rules and the manufacturing need to maintain predictable yield. The design rules for each technology node are a result of a careful tradeoff

AKI FUJIMURA, is Chairman and CEO of D2S, Inc., San Jose, CA.

LITHOGRAPHY

among many different, often competing, factors.

Wafer CDU is one factor that has always been important to the establishment of design rules. Wafer CDU is a measure of the statistical variation, often expressed as a standard deviation, of CD when a given feature is repeated many times on a wafer. Lower variation in CD is better; however, it is always a tradeoff. Each wafer CDU degradation is met with consequences in terms of design rules.

Poor wafer CDU forces more margin into design rules to account for the possibility that a particular instance could be manufactured too large or too small. For example, a spacing rule between features may need to be broadened to avoid bridging adjacent features on the finished wafer. Or, a minimum feature size may need to be larger to account for the possibility that an instance of that feature could be too narrow once manufactured, causing an open circuit.

As an example, the inability to maintain tight control on wafer CDU at advanced nodes has caused redundant contacts and vias to be required in order to maintain yield. Because contacts and vias are the smallest-sized features in both the X and Y dimensions to write on a wafer, they are the hardest to yield predictably. Design rules have already been modified to require techniques such as double vias to account statistically for poor CDU on single vias. Double contacts and vias negatively impact chip area, and therefore the performance of, and the power required to implement, a given functionality.

Wafer CDU is impacted by a variety of factors, including lithography performance, and therefore the quality of optical proximity correction (OPC). For the first time, wafer CDU for the sub-20nm logic nodes is also significantly affected by shape-dependent mask CDU.

Shape-dependent mask CDU and wafer quality

Shape-dependent mask CDU has become a topic of increasing concern because mask shapes are becoming increasingly complex (less rectangular, and more an orthogonal approximation of a curvilinear shape), and mask patterns are now approaching critical sub-80nm dimensions.

The ability to use ideal (i.e., truly curvilinear) ILT shapes on masks, rather than Manhattan approxima-

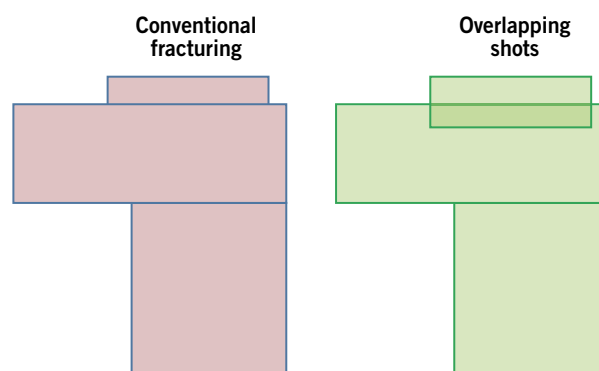


FIGURE 2. When creating the feature shown above, conventional fracturing cannot avoid slivers (left). Allowing overlapping shots eliminates the need for sliver shots to produce complex mask shapes in most cases (right).

tions, has been shown to yield better wafer quality [1]. Previously, it had been assumed that ideal ILT shapes were not practical because such shapes could not be written on the mask within reasonable write times. While this was and still is true for conventional fracturing approaches, recently introduced MB-MDP techniques enable the writing of ideal ILT shapes on the mask in write-times equivalent to those needed to write complex “Manhattanized” shapes that are fractured conventionally. This new mask-data preparation technology enables the use of ideal ILT shapes to optimize the wafer performance. The remaining problem with these types of shapes, especially at smaller process nodes, is shape-dependent mask CDU.

Even with purely orthogonal Manhattanized shapes, when the orthogonal jogs in the shape outline become smaller, the actual shape written on the mask becomes more and more curvilinear. This natural rounding effect is due to forward-scattering of VSB-based mask writing. This rounding always causes 90-degree corners and thin features to have poor dose margin, which results in poor mask CDU. Complex SRAFs, whether Manhattanized or ideal, are a combination of both of these “problem” shapes and so introduce the shape-dependent mask CDU issue at the 20nm logic node and below.

In mask writing, there are three principal issues that contribute to CDU problems: dose margin, slivers and CD split. All three issues are shape-dependent with complex Manhattanized or ideal mask shapes. And all

three issues are reduced with MB-MDP techniques.

Dose Margin In VSB-based e-beam writing, dose margin is used to model a collective effect of various sources of manufacturing variation, including variations in e-beam current or dose as well as resist conditions such as sensitivity, distance, thickness and temperature. Good dose margin makes mask shapes resilient to these sources of variation. Conversely, poor dose margin makes shapes more vulnerable to variation.

At the 20nm-and-below process nodes, mask patterns are approaching sub-80nm dimensions. e-beam writing is less predictably accurate as feature sizes drop below 80nm, an effect that is commonly referred to as the “linearity” problem. But in addition, there is a dose margin problem, and therefore a CDU problem. Specifically, there is a shape-dependent CDU problem.

Previously, most mask shapes were orthogonal and VSB shots were larger than 100nm in one dimension. Because 100nm is sufficiently larger than the forward scattering radius of the e-beam and its effects on the resist, the dose margin of CDs (almost always measured orthogonally) was stable across different shapes on the mask. Dose margin was still an important criterion, but the issues at this point came mostly from backscatter correction, also called proximity effect correction (PEC). A large amount of backscatter would produce poor dose margin, so areas that are dense or opaque masks would have worse dose margin. However, the issue was fairly uniform across all mask shapes.

Now that mask shapes have smaller features, and more and more of the mask is written with the corners of the VSB shots, the dose margin issue has become shape dependent.

As shown in **Fig. 1**, a drawn 90nm x 45nm rectangle (top left) will appear on the mask as an oval (top center). The width will be unreliable because the dose margin is relatively poor in that dimension, as illustrated by the red color (top right).

However, if the same 90nm x 45nm shot was repeated in a stair-step fashion (bottom left) to create an approximately diagonal line (bottom center), the dose margin, and therefore the CD, of that diagonal line is acceptable (bottom right). The two extreme ends of the line still have poor dose margin, but that direction is not likely to be the CD for this kind of shape, and the impact to the area of the mask shape is less significant. For features sized below 80nm for VSB-based mask writing, dose margin is shape dependent. Therefore, for these features, CDU is also shape dependent.

Slivers Using the VSB approach, there is a small but unavoidable error introduced because the first beam aperture and the second beam aperture are overlapped to “cut” the rectangular VSB shot. This small error in the X and Y dimensions, as well as in angular distortion, becomes much greater for small shots, where the error represents a greater proportion of the shot. This is particularly pronounced for narrow shots with a high aspect ratio. This is often referred to as the “sliver” issue. As shown in **Fig. 2**, allowing overlapping shots can eliminate the need for sliver shots to produce the desired shape.

CD Split Another source of CD variation is CD split[2], a condition that occurs when two or more distinct VSB shots define the measured CD. CD split is a CDU issue because positional variation translates to CD variation where there is CD split. Masks with only rectangular shapes minimize CD split. Masks with complex shapes (whether ideal curvilinear or

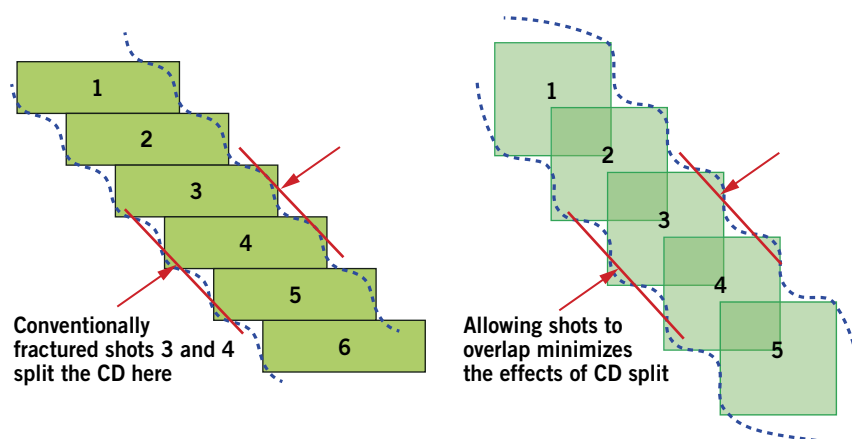


FIGURE 3. CD split can be reduced by overlapping e-beam shots.

LITHOGRAPHY

Manhattanized approximations) have significant CD split issues if conventionally fractured. Allowing overlapping shots substantially reduces the CD split problem, as seen in **Fig. 3** below. The use of circular e-beam shots is even more effective for reducing the CD split problem, as shown in **Fig. 4**.

All three major contributors to mask CDU—dose margin, slivers and CD split—are shape dependent. All three are improved with new techniques that are enabled by MB-MDP.

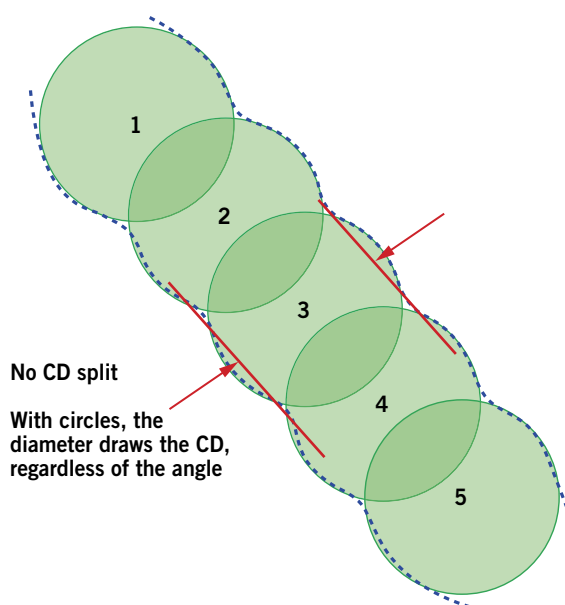


FIGURE 4. Because the diameter of a circle draws the CD regardless of the angle, circular e-beam shots are even more effective for reducing CD split.

New mask manufacturing technologies

Since the introduction of VSB mask writing, the range of technologies used in mask manufacturing has remained fairly static. Today, in response to the challenges posed by the 20nm-and-below process nodes, new mask manufacturing techniques such as MB-MDP, MPC, dose modulation and circular-shaped and overlapping e-beam shots offer distinct advantages. All impact shape-dependent mask CDU, which in turn improves design rules and/or wafer quality.

MB-MDP is a new, model-based mask-data preparation technology. Traditional fracturing techniques for mask data preparation look at the desired drawn shape

and find the combination of adjacent (non-overlapping) rectangles (and potentially some triangles) that will create those shapes. In contrast, MB-MDP is based on mask simulation. By fully simulating the energy deposited on the mask by each e-beam shot, MB-MDP is able to match shapes much more flexibly. MB-MDP can use any shape aperture (including circles), it can overlap these shots and it can assign a dosage level to each shot. The end result is better mask accuracy in terms of both faithful reproduction of each shape and manufacturing variation.

In addition, because MB-MDP simulates the effects of shots on the mask plane and produces the desired contour at the resist threshold, MB-MDP provides built-in MPC. Much as OPC corrects lithographic process effects, MPC corrects mask process effects such as fogging, development and etch loading, and e-beam proximity effects[3]. MPC also can be used to correct the size of mask features less than 80nm wide that are impacted by e-beam errors.

Until now, all shots have been considered to be “full strength” for mask-data preparation purposes. However, dose modulation helps to improve CDU of sub-80nm features that would otherwise print smaller than intended[4]. Oversizing the data (purposefully drawing larger shapes with the knowledge that they will write smaller on the mask) can also correct small shapes, but the dose margin will not be as good as compared to increasing the dose. The capability to have per-shot dose control gives more flexibility with less impact on mask write-times.

The newly introduced ability to use circular apertures in VSB stencils has a number of benefits. First, the use of circular shots to create contacts and vias improves depth of focus and CDU for these critical and ubiquitous features.[5] Next, the use of circular shots to create complex mask features such as curvilinear SRAFs reduces shot-count significantly for these shot-intensive features.[6] Finally, circles have also been demonstrated to improve shape-dependent CDU for advanced masks.[7]

While this new generation of mask manufacturing technologies is still in development, many have been demonstrated through industry collaborations to improve shape-based CDU[8]. Some of these emerging technologies are already available for limited

commercial use, and others are in the process of commercial implementation.

Conclusion

As process technologies approach 20nm-and-below nodes, the application of new mask manufacturing technologies such as MB-MDP, MPC, dose modulation and circular shots can have critical influence on shape-dependent mask CDU, which in turn impacts design rules and/or wafer quality. More than ever before, the mask manufacturing techniques used for any given design can now have far-reaching impact on the output of the entire design-to-manufacturing chain.

Moving forward, process development teams will need to consider shape-dependent mask CDU, and the enablement of complex, even ideal ILT, patterns as critical factors for reducing the tradeoffs between improving wafer yield and tightening design rules. Design teams will benefit from more liberal design rules enabled by the tighter control of shape-dependent mask CDU afforded by these new mask-manufacturing techniques. Likewise, wafer manufacturers will benefit from the increased wafer quality and yield provided by masks with better shape-dependent mask CDU. ♦

References

1. Timothy Lin, Emile Sahouria, Nataraj Akkiraju, Steffen Schulze, "Reducing shot count through optimization based fracture," *Proc. SPIE 8166* (2012).
2. Ryan Pearman, Robert Pack, "MB-MDP enables circular shots to improve mask accuracy as well as shot count," Whitepaper, D2S, Inc., February 13, 2012.
3. G. Chen, J-S. Wang, S. Bai, R. Howell, J. Wiley, A. Vacca, T. Kurosawa, T. Nishibe, T. Takigawa, "Model based short range mask process correction," *PMJ* 2008.
4. Aki Fujimura, "Model-based mask data preparation using overlapping shots: making optical lithography cost-effective for 20-nm devices," Whitepaper, eBeam Initiative, 2011.
5. Aki Fujimura, "Circles: one key to successful lithography at advanced nodes," Whitepaper, eBeam Initiative, 2010.
6. Ibid.
7. Ibid.
8. Pearman, Pack, op cit

ad index

Advertiser	Pg
Indium Corp.....	7
Julabo USA, Inc.	9
SEMI.....	5
Solid State Equipment LLC	C2
Stanford Research Systems.....	3
The Confab	C3
Verity Instruments, Inc.....	C4

The Advertiser's Index is published as a service. The publisher does not assume any liability for errors or omissions.

Solid State TECHNOLOGY

EXECUTIVE OFFICES

PennWell, 98 Spit Brook Rd,
Nashua, NH 03062-5737
Tel: 603/891-0123

ADVERTISING

Marcella Hanson—

Ad Traffic Manager

Justine Eversman—

Marketing Communications
Manager

ADVERTISING

SALES OFFICES

Group Publisher

Susan Smith

98 Spit Brook Rd, Nashua,
NH 03062-5737
Tel: 603/891-9447;
Fax: 603/891-9328;
e-mail:
susans@pennwell.com

Sales Manager

Kerry Hoffman

98 Spit Brook Rd. Nashua,
NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: kerryh@pennwell.com

The ConFab

Sabrina Straub

98 Spit Brook Rd. Nashua,
NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: sabrinas
@pennwell.com

Austria, Germany,
Liechtenstein, Russia,
N. Switzerland,
Eastern Europe

Holger Gerisch

Hauptstrasse 16,
D-82402 Seeshaupt,
Germany;
Tel: 49/8801-302430;
Fax: 49/8801-913220;
e-mail: holgerg@pennwell.com

France, Netherlands,
Belgium, W. Switzerland,
Spain, Greece, Portugal

Luis Matutano

Adecome+
1, rue Jean Carasso,
F-95870 Bezons, France
Tel: 33/1-30 76 55 43;
Fax: 33/1-30 76 55 47;
e-mail: luism@pennwell.com

United Kingdom
& Scandinavia

Kerry Hoffman

98 Spit Brook Rd. Nashua,
NH 03062-5737
Tel: 603/891-9118;
Fax: 603/891-9328;
e-mail: kerryh@pennwell.com

Israel

Dan Aronovic

Allstar Media Inc.,
3/1 Hatavos St., Kadima,
60920, Israel
Tel / Fax: 972/9-899-5813
e-mail: aronovic@aactcom.co.il

Japan

Masaki Mori

ICS Convention Design, Inc.,
Chiyoda Bldg.,
Sarugaku-cho 1-5-18,
Chiyoda-ku, Tokyo
101-8449, Japan
Tel: 3-3219-3641;
Fax: 3-3219-3628;
e-mail: mori-masaki@ics-
inc.co.jp

Taiwan

Diana Wei

Arco InfoComm, 4F-1, #5
Sec. 1 Pa-Te Rd. Taipei,
Taiwan R.O.C. 100
Tel: 866/2-2396-5128
Ext. 270
e-mail: diana@arco.com.tw

China, Hong Kong

Adonis Mak

ACT International, Unit B, 13/F,
Por Yen Building, 478 Castle
Peak Road, Cheung Sha Wan,
Kowloon, Hong Kong
Tel: 852/2-838-6298;
Fax: 852/2-838-2766;
e-mail: adonism@
actintl.com.hk

List Rental

Kelli Berry

1421 South Sheridan Rd.,
Tulsa, OK 74112;
Tel: 918/831-9782; Fax:
918/831-9758;
e-mail: kelli@pennwell.com

September 2012, Volume 55, Number 7 • **Solid State Technology** ©2012 (ISSN 0038-111X) Periodicals postage paid at Tulsa, OK 74112, & additional mailing offices. Published 9x per year (Jan, Mar, Apr, May, Jun, Jul, Sep, Oct and Nov) by PennWell Corp., 1421 S. Sheridan Rd., Tulsa, OK 74112. **Subscriptions:** Domestic: one year: \$258.00, two years: \$413.00; one year Canada/Mexico: \$360.00, two years: \$573.00; one-year international airmail: \$434.00, two years: \$691.00; Single copy price: \$15.00 in the US, and \$20.00 elsewhere. Digital distribution: \$130.00. You will continue to receive your subscription free of charge. This fee is only for air mail delivery. Address correspondence regarding subscriptions (including change of address) to: **Solid State Technology**, PO Box 3425, Northbrook, IL 60065-9595, sst@omeda.com, ph 847-559-7500 (8 am – 5 pm, CST). PRINTED IN THE USA. GST NO. 126813153. Publication Mail Agreement No. 40052420. **POSTMASTER:** Send address changes to **Solid State Technology**, PO Box 3425, Northbrook, IL 60065-9595. Return Undeliverable Canadian Addresses to: P.O. Box 122, Niagara Falls, ON L2E 6S4.

Nanoimprint lithography's role in 450mm

During SEMICON West in July 2012 there was increased momentum and growing industry consensus on the timing for the 450mm wafer transition. This broad support is a necessary milestone that helps mitigate risk but it does not guarantee timely innovation. Coordinating the 450mm wafer size transition with Moore's Law has never been more complicated, especially for advanced lithography. Equipment companies are not eager to repeat the 'bridge tool' mistakes of the 300mm transition, yet 193i has all but reached the end of its resolution roadmap (forcing adoption of self-aligned multiple patterning schemes) and EUV remains elusive. While the industry is addressing this conundrum by hedging on both these optical technologies, neither solves the immediate problem of orchestrating an efficient 450mm wafer transition. Developing tools for the future (etch, deposition, CMP, metrology, etc.) require patterns from the future on 450mm wafers today. Fortunately, nanoimprint lithography has made impressive progress over the last twelve months and is currently being groomed for advanced FLASH production with 300mm system installations at two of the largest

semiconductor memory manufacturers.

Consequently, Molecular Imprints Inc. (MII) was awarded a contract in November 2011 from a leading IC manufacturer for the industry's first 450mm lithography tool. The advanced patterned large wafers from this tool will support the development of the industry's 450mm equipment solution beginning in Q4'2012.

In selecting a 450mm lithographic technology for these critical test wafers several factors such as resolution, extensibility, cost and availability were considered. EUV's protracted technical challenges and associated costs eliminated it as a viable option while 193i lithography did not satisfy the near-term 450mm availability and long-term resolution requirements. Fortunately imprint lithography has recently made significant progress and is able to meet all of these requirements. Molecular Imprints Jet and Flash™ (J-FIL™) technology has shown its flexibility to adapt to a variety of substrate sizes from 65mm hard disk drive platters to the

Nanoimprint is the only lithography that is currently capable of syncing the future's advanced patterned features with the pending 450mm substrate transition

much larger flat panel displays substrates. J-FIL is being slated for advanced semiconductor pilot-lines in the next 18 to 24 months by early adopters in an effort to stem rising costs and schedule risks of optical lithography.

Several equipment companies have opted to baseline J-FIL on their existing platforms using 300mm wafers. Once their imprinted pattern transfer processes have been characterized on 300mm tools then any identified imprint nuances can be decoupled from their specific 450mm form factor challenges. We expect this baseline activity to be very straight forward as J-FIL resist is very similar to 193 resists. Molecular Imprints intends to provide 300mm patterned wafer services in Q4'2012 that will closely correlate (in terms of mask designs and imprint process conditions) to the actual 450mm J-FIL platform.

In summary, nanoimprint is the only lithography that is currently capable of syncing the future's advanced patterned features with the pending 450mm substrate transition. Early access to these advanced test wafers is paramount for equipment companies to efficiently develop their 450mm toolsets without neglecting Moore's Law. The low cost and extensibility of J-FIL lithography provides a long technology roadmap for advanced memory manufacturers while enabling the broader semiconductor industry to begin its 450mm initiative. ♦



PAUL HOFEMANN VP
Corporate Marketing
and Business
Development,
Molecular Imprints,
phofemann@molec-
ularimprints.com



Many **thanks** to the attendees, speakers and sponsors who made Solid State Technology's 8th annual ConFab a resounding success in 2012. We look forward to another great event in 2013!

We would like to acknowledge the following organizations who took part in The ConFab 2012:

ABB
ACT International
Advanced Semiconductor Manufacturing Corp. (ASMC)
Advantest
AG Semiconductor Services
Amkor Technology
Applied Materials Inc.
Applied Seals North America Inc.
ASE Inc.
ATMI
AZ Electronic Materials
Brewer Science
Carl Zeiss
CH2M HILL
CSMC Technologies Corp.
Dai Nippon Printing Co.
Edwards
EV Group
Freescale Semiconductor
G450 Consortium
GLOBALFOUNDRIES
Hattori Consulting International
Hitachi High Technologies America
Hitech Semiconductor (Wuxi) Co.

IBM Corp.
imec
Infineon Technologies Dresden GmbH
Intel Capital
Intel Corp.
International Rectifier
KeyAssets
KLA-Tencor
Lam Research
Levitronix
LORD Corporation
LSI Corp.
Marcy NanoCenter at SUNYIT & NY
Loves Nanotech
MEMSCAP, Inc.
Multitest
Nikon Precision
Nvidia Corp.
ON Semiconductor Corp.
ON Semiconductor Philippines, Inc.
Pall Microelectronics
PennWell Corp.
Qcept Technologies
Qualcomm Inc.
Renesas Electronics America

Rudolph Technologies
Rygler & Associates
SEMATECH
SEMATECH Manufacturing Initiative (SMI).
SEMI
Semico Research Corp.
Semiconductor Manufacturing International Corp. (SMIC)
Shanghai Belling Co.
Shanghai Hua Hong NEC Electronics Co.
SICA
Solid State Technology
SPG Applied Global Services
Technology Connexions
Tokyo Electron America
TSMC
ULVAC Technologies
Valqua America Inc.
VIA Technologies, Inc.
VLSI Research Co.
X-FAB Texas, Inc.
Xilinx, Inc.
ZYadS Inc.

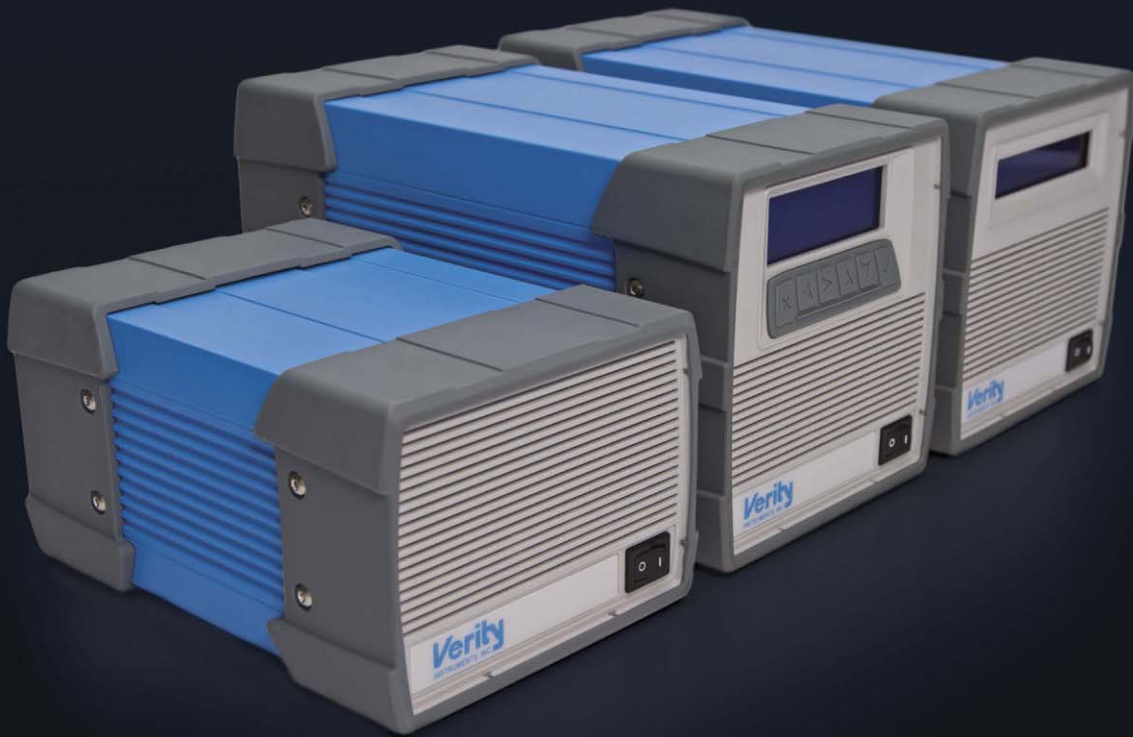
The ConFab will be back at the Encore at the Wynn Las Vegas June 23-26, 2013.

Be part of the collaborative event that provides intensive manufacturing-centric discussions, idea exchange and alliance-building, and private boardroom meetings for the semiconductor manufacturing and supplier community. To learn more about what was presented at our 2012 event and hear from some of the attendees, visit <http://bit.ly/PpcZSO>

Semiconductor Device Manufacturing, Foundry, and Fabless Executives: Visit www.theconfab.com to pre-register and pre-qualify to attend as our VIP guest.

Semiconductor Equipment and Material Suppliers: If you would like to participate as a sponsor for this unique event, please contact **Sabrina Straub** at +1 603 891 9213 or sabrinass@pennwell.com.

We've gone the extra mile so you don't go the extra nanometer.



THE NEXT GENERATION HAS ARRIVED.

Introducing the latest additions to the Verity family of smart spectrometers featuring the SD1024X, a new industry standard that combines spectrometer and PC in the same space, eliminating the need for a dedicated applications computer. The new SD1024G Series delivers improved capability with industry leading ultra-performance, general purpose, and high resolution model options. Coupled with the compact FL2100 flashlamp module the new series addresses the broadest range of challenging plasma and film thickness/etch depth endpoint control problems. Now, more than ever, the first name in endpoint detection is the last word in performance.

Learn more at www.Verityinst.com.

Verity

INSTRUMENTS, INC.