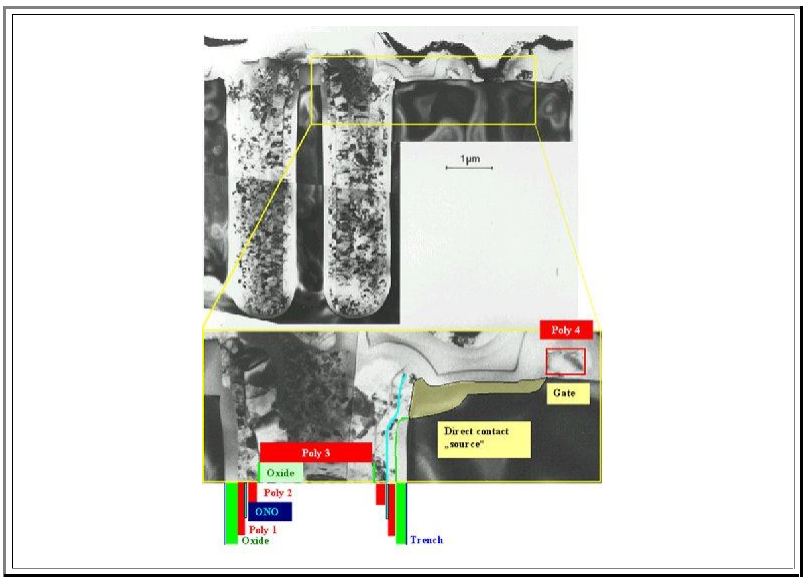
6.2.3 CVD for Poly-Silicon, Silicon Nitride and Miscellaneous Materials

Poly Silicon CVD

- If we were to use an epitaxial reactor for wafers covered with oxide, a layer of **Si** would still be deposited on the hot surface - but now it would have no "guidance" for its orientation, and poly-crystalline **Si** layers (often just called "**poly**" or "polysilicon") would result.
  - **Poly-Si** is one of the key materials in microelectronics, and we know already how to make it: Use a **CVD** reactor and run a process similar to epitaxy.
  - If doping is required (it often is), admit the proper amounts of dopant gases.
- However, we also want to do it cheap, and since it we want a polycrystalline layer, we don't have to pull all the strings to avoid crystal lattice defects like for epitaxial **Si** layers.
  - We use a more simple **CVD** reactor of the furnace type shown for oxide **CVD**, and we employ smaller temperatures (and low pressure, e.g. **60 Pa** since we only need thin layers and can afford lower deposition rates). This allows to use SiH_4 instead of$SiCl_4$; our process may look like this:

$$SiH_4 \xrightarrow[630^oC]{60\ Pa} Si + 2\ H_2$$

  - Much cheaper! The only (ha ha) problem now is: Cleaning the furnace. Now you have poly-**Si** all over the place; a little bit nastier than SiO_2, but this is something you can live with.
- What is poly-**Si** used for and why it is a key material?
  - Lets look at a **TEM** (=transmission electron microscope) picture of a memory cell (transistor and capacitor) of a **16 Mbit DRAM**. For a larger size picture and additional pictures click here.



- All the speckled looking stuff is poly-**Si**. If you want to know exactly what you are looking at, turn to the drawing of this cross section. We may distinguish **4** layers of poly **Si**:
  - "*Poly **1***" coats the inside of the trench (after its surface has been oxidized for insulation) needed for the capacitor. It is thus one of the "plates" of the capacitor. In the **4 Mbit DRAM** the substrate **Si** was used for this function, but the space charge layer extending into the **Si** if the capacitor is charged became too large for the **16 Mbit DRAM**.
  - The "*Poly **2***" layer is the other "plate" of the capacitor. The **ONO** dielectric in between is so thin that it is practically invisible. You need a ***HRTEM*** - a high resolution transmission electron microscope - to really see it.
  - Now we have a capacitor folded into the trench, but the trench still needs to be filled. Poly-**Si** is the material of choice. In order to insulate it from the poly capacitor plate, we oxidize it to some extent before the "*poly **3***" plug is applied.
- One plate of the capacitor needs to be connected to the source region of the transistor. This is "simply" done by removing the insulating oxide from the inside of the trench in the right place (as indicated).
  - Then we have a *fourth poly layer*, forming the gates of the transistors.
  - And don't forget: there were two sacrificial poly-**Si** layers for the LOCOS process!
- That makes **6** poly-**Si** deposition (that we know of). Why do we like poly-**Si** so much?

- Easy! It is perfectly compatible with single crystalline **Si**. Imagine using something else but poly-**Si** for the plug that fills the trench. If the thermal expansion coefficient of "something else" is not quite close to **Si**, we will have a problem upon cooling down from the deposition temperature.
- No problem with poly. Moreover, we can oxidize it, etch it, dope it, etc. (almost) like single crystalline **Si**. It only has *one* major drawback: Its conductivity is not nearly as good as we would want it to be. That is the reason why you often find the poly-gates (automatically forming one level of wiring) "re-enforced" with a **silicide** layer on top.
- A silicide is a metal silicon compound, e.g. **Mo_2Si**, **PtSi**, or **Ti_2Si**, with an almost metallic conductivity that stays relatively inert at high temperatures (in contrast to pure metals which react with **Si** to form a silicide). The resulting double layer is in the somewhat careless slang of microelectronics often called a "*polycide*" (its precise grammatical meaning would be the killing of the poly - as in fratricide or infanticide).
- Why don't we use a silicide right away, but only in conjunction with poly-**Si**? Because you would loose the all-important high quality interface of (poly)-**Si** and **SiO_2**!

Si_3N_4 Deposition

- We have seen several uses for silicon nitride layers - we had **LOCOS**, **FOBIC** (and there are more), so we need a process to deposit **Si_3N_4** .
  - Why don't we just "nitride" the **Si**, analogous to oxidations, by heating the **Si** in a **N_2** environment? Actually we do - on occasion. But **Si_3N_4** is so impenetrable to almost everything - including nitrogen - that the reaction stops after a few **nm**. There is simply no way to grow a "thick" nitride layer thermally.
  - Also, don't forget: **Si_3N_4** is always producing tremendous stress, and you don't want to have it directly on the **Si** without a buffer oxide in between. In other words: We need a **CVD** process for nitride.
- Well, it becomes boring now:
  - Take your **CVD** furnace from before, and use a suitable reaction, e.g.
    .

$$3\,SiH_2Cl_2 + 4NH_3 \Rightarrow Si_3N_4 + 2HCl + 1{,}5\,H_2 \quad (\approx 700\,^{o}C))$$

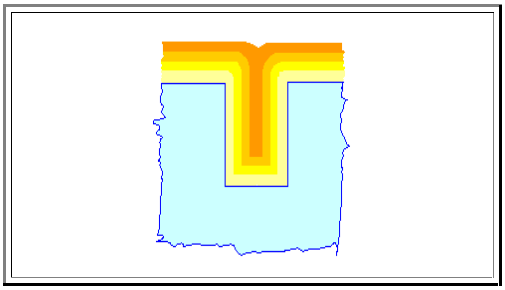
  - Nothing to it - except the cleaning bit. And the mix of hot ammonia (**NH_3**) and **HCl** occurring simultaneously if you don't watch out. And the waste disposal. And the problem that the layers, being under internal stresses, might crack upon cooling down. And, - well, you get it!

Tungsten CVD

- For reasons that we will explain later, it became necessary at the end of the eighties, to deposit a metal layer by **CVD** methods. Everybody would have loved to do this with **Al** - but there is no good **CVD** process for **Al**; nor for most other metals. The candidate of choice - mostly by default - is **tungsten** (chemical symbol ***W*** for "Wolfram").
  - Ironically, **W-CVD** comes straight form nuclear power technology. High purity **Uranium** (chemical symbol ***U***) is made by a **CVD** process not unlike the **Si** Siemens process using **UF_6** as the gas that decomposes at high temperature.
  - W is chemically very similar to **U**, so we use **WF_6** for **W-CVD**.
- A **CVD** furnace, however, is not good enough anymore. **W-CVD** needed its own equipment, painfully (and expensively) developed a decade ago.
  - We will not go into details, however. **CVD** methods, although quite universally summarily described here, are all rather specialized and the furnace type reactor referred to here, is more an exception than the rule.

Advantages and Limits of CVD Processes

- **CVD** processes are ideally suited for depositing thin layers of materials on some substrate. In contrast to some other deposition processes which we will encounter later, **CVD** layers always follow the contours of the substrate: They are conformal to the substrate as shown below.



- Of course, conformal deposition depends on many parameters. Particularly important is which process dominates the reaction:
  - *Transport controlled process* (in the gas phase). This means that the rate at which gas molecules arrive at the surface controls how fast things happen. This implies that molecules react immediately wherever they happen to reach the hot surface. This condition is always favored if the *pressure is low enough*.
  - *Reaction controlled kinetics*. Here a molecule may hit and leave the surface many times before it finally reacts. This reaction is dominating at high pressures.
- Controlling the partial pressure of the reactants therefore is a main process variable which can be used to adjust layer properties.
  - It is therefore common to distinguish between ***APCVD*** (**=** atmospheric pressure **CVD**) and ***LPCVD*** (**=** low pressure **CVD**).
  - **LPCVD**, very generally speaking, produces "better" layers. The deposition rates, however, are naturally much lower than with **APCVD**.
- **CVD** deposition techniques, though quite universal and absolutely essential, have certain *disadvantages*, too. The two most important ones (and the only ones we will address here) are
  - They are not possible for some materials; there simply is no suitable chemical reaction.
  - They are generally not suitable for *mixtures* of materials.
- To give just one example: The metallization layers for many years were (and mostly still are) made from **Al** - with precise additions of **Cu** and **Si** in the **0,3% - 1%** range
  - There is no suitable **Al**-compound that decomposes easily at (relatively low) temperatures. This is not to say that there is none, but all **Al**-organic chemicals known are too dangerous to use, to expensive, or for other reasons never made it to production (people tried, though).
  - And even if there would be some **Al CVD** process, there is simply no way at all to incorporate **Si** and **Cu** in the exact quantities needed into an **Al CVD** layer (at least nobody has demonstrated it so far).
- Many other materials, most notably perhaps the silicides, suffer from similar problems with respect to **CVD**. We thus need alternative layer deposition techniques; this will be the subject of the next subchapter.

Footnote:	The name "*Poly Silicon*" is used for at least three qualitatively very different kinds of materials:
	1. The *"raw material" for crystal growth*, coming from the "Siemens" **CVD** process. It comes - after breaking up the rods - in large chunks suitable for filling the crucible of a crystal grower.
	2. Large ingot of cast **Si** and the *thin sheets made from them*; exclusively used for solar cells. Since the grains are very large in this case (in the cm range), this material is often referred to as "**multi crystalline Si**".
	3. The *thin layers of poly **Si*** addressed in this sub-chapter, used for micro electronics and micro mechanical technologies. Grain sizes then are µm or less.
	In addition, the term poly **Si** might be used (but rarely is) for the *dirty stuff coming out of the **Si** smelters*, since this **MG-Si** is certainly poly-crystalline