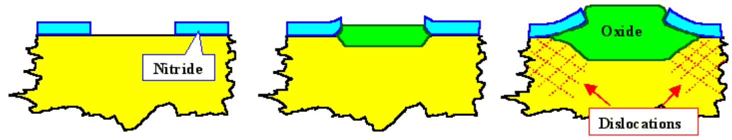
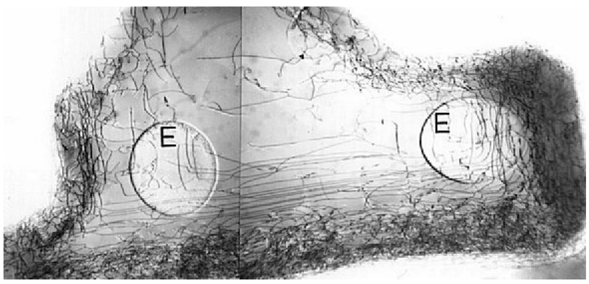
6.1.2 LOCOS Process

Basic Concept of Local Oxidation

- The abbreviation "***LOCOS***" stands for "**Local Oxidation of Silicon**" and was almost a synonym for **MOS** devices, or more precisely, for the insulation between single transistors. **LOCOS** makes the isolation between **MOS** transistors considerably easier then between bipolar transistors, cf. the drawings discussed before:
  - For bipolar transistors, you have to separate the collectors. This involves an epitaxial layer and some deep diffusion around every transistor.
  - For MOS transistors, no isolation would be needed weren't it for the possible parasitic transistors. And this problem can be solved by making the "gate oxide" of the parasitic transistors - which then is called **field oxide** - sufficiently thick.
- The thick field oxide has been made by the **LOCOS** process from the beginning of **MOS** technology until presently, when **LOCOS** was supplanted by the "box isolation technique", also known as "***STI***" for "**Shallow trench isolation**".
  - Since the **LOCOS** technique is still used, and gives a good example of how processes are first conceived, are optimized with every generation, become very complex, and are finally supplanted with something different, we will treat it here in some detail
- As the name implies, the goal is to oxidize **Si** only *locally*, wherever a field oxide is needed. This is necessary for the following reason:
  - *Local* (thermal) oxide penetrates into the **Si** (oxidation is using up **Si**!), so the **Si** - SiO_2 interface is *lower* than the source - drain regions to be made later. This could not be achieved with oxidizing all of the **Si** and then etching off unwanted oxide.
  - For device performance reasons, this is highly beneficial, if not absolutely necessary.
- For a *local* oxidation, the areas of the **Si** that are not to be oxidized must be protected by some *material* that does not allow oxygen diffusion at the typical oxidation temperatures of **(1000 - 1100) ^{0}C**. We are talking electronic materials again!
  - The *only material* that is "easily" usable is **Silicon nitride**, Si_3N_4. It can be deposited and structured without too much problems and it is compatible with **Si**.
  - However, Si_3N_4 introduces a major new problem of its own, which can only be solved by making the process more complicated by involving yet another materials. This gives a ***succinct*** example of the statement made before: That materials and processes have to be seen as a unit.
  - Lets see what would happen with just a Si_3N_4 layer protecting parts of the **Si** from thermal oxidation.



  - Oxygen diffusion through the oxide already formed would also oxidize the Si under the Si_3N_4; i.e. there would be some amount of lateral oxidation. Since a given volume of **Si** expands by almost a factor of **2** upon oxidation (in other words: Oxidizing **1cm^3** of **Si** produces almost **2 cm^3** of SiO_2), the nitride mask is pressed upwards at the edges as illustrated.
  - With increasing oxidation time and oxide thickness, pressure under the nitride mask increases, and at some point the *critical yield strength* of **Si** at the oxidation temperature is exceed. *Plastic deformation* will start and dislocations are generated and move into the **Si**. Below the edges of the local oxide is now a high density of dislocations which kill the device and render the **Si** useless - throw it out.
  - This is not "theory", but eminently practical as shown in the ***TEM*** picture from the early days of integrated circuit technology:



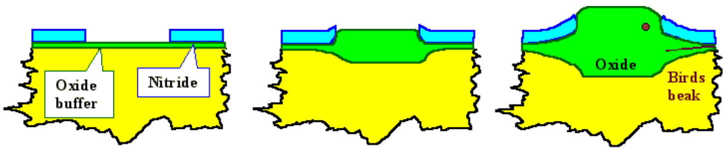
- We are looking through a piece of **Si**. The dark lines are the projections of single dislocations, the "dislocations tangles" corresponds to oxide edges; "**E**" shows contact areas (emitters) to the **Si**. Another picture can be found in the link.
- Actually, it doesn't even need the oxidation to produce dislocations. **Si_3 N_4** layers are always under large stresses at room temperature and would exert great shear stresses on the **Si**; something that can not be tolerated as soon as the nitride films are more than a few **nm** thick.

We arrive at a simple rule: You *cannot* use **Si_3 N_4** directly on **Si** - never ever. What are we to do now, to save the concept of local oxidation?

Buffer Oxide

We need something *between* the **Si_3 N_4** mask and the **Si**; a thin layer of a material that is compatible with the other two and that can *relieve the stress* building up during oxidation. Something like the oil in you motor, a kind of ***grease***.

- This "grease" material is **SiO_2**, as you might have guessed - it was already mentioned before under its proper name of "**buffer oxide**". The hard **Si_3 N_4** (which is a ceramic that is very hard not yielding at a "low" temperature of just about **1000 ^oC**), is now pressing down on something "soft", and the stress felt by the **Si** will not reach the yield stress - if everything is done right.
- The situation now looks like this



- No more dislocations, but a comparatively large lateral oxidation instead, leading to a configuration known as "**birds beak**" for the obvious reason shown in the picture to the right (the inserts just are there to help you see the bird).

So we got rid of one problem, but now we have another one: The lateral extension of the field oxide via the birds beak is comparable to its thickness and *limits the minimum feature size*.

- While this was not a serious problems in the early days of **IC** technology, it could not be tolerated anymore around the middle of the eighties.
- One way out was the use of a poly-**Si** layer as a sacrificial layer. It was situated on top of the buffer oxide below the nitride mask and was structured with the mask. It provided some sacrificial **Si** for the "birds beak" and the total dimension of the field oxide could be reduced somewhat.
- This process is shown in comparison with the standard process in the link.

But even this was not good enough anymore for feature sizes around and below **1 µm**. The **LOCOS** process eventually became a very complicated process complex in its own right; for the Siemens **16 Mbit DRAM** it consisted of more than **12** process steps including:

- **2** oxidations, **2** poly-**Si** deposition, **1** lithography, **4** etchings and **2** cleaning steps.
- It was one of the decisive "secrets" for success, and we can learn a simple truth from this:

Before new materials and processes are introduced, the existing materials and processes are driven to extremes! And that is not only true for the **LOCOS** process, but for all other processes.

- Still, with feature sizes shrinking ever more, **LOCOS** reached the end of its useful life-span in the nineties and had to be replaced by "Box isolations", a simple concept in theory, but hellishly difficult in reality.
- The idea is clear: Etch a hole (with vertical sidewalls) in the **Si** wherever you want an oxide, and simple "fill" it with oxide next. More about this process can be found in the link above.