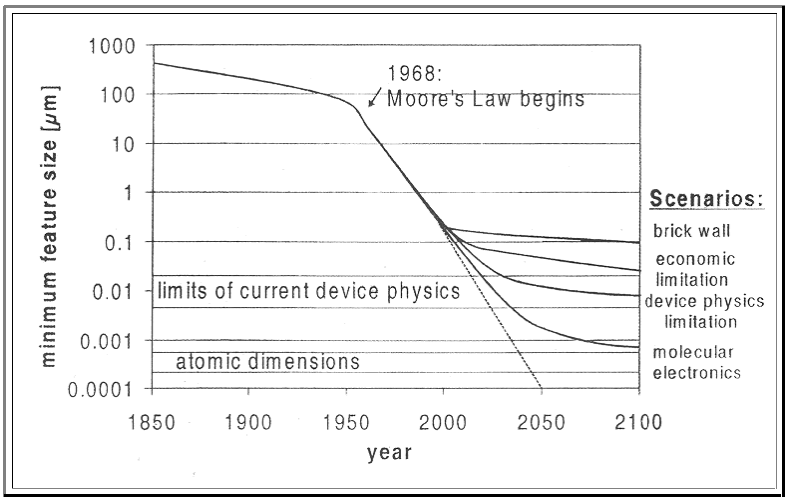
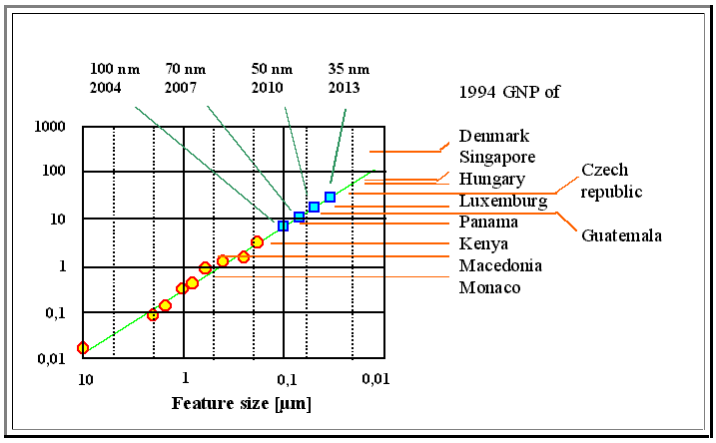
Moore's Law: Break Down Scenarios

Illustration

- Here is an illustration of **Moore's Law** with several scenarios for possible extrapolations.



- The dashed line shows the linear extrapolation. It is sure to break down - at the very last when feature size come down to the level of atoms
  - The "molecular electronics" scenario thus must be seen as the best possible case and would keep us going for another **20 - 30** years.
  - On the other extreme, the "Brick wall" scenario assumes that technology simply hits an insurmountable barrier right now. In other words, feature sizes will not come below about **0,1 µm** ever. The end then would be near.
  - In between are scenarios where feature size reduction is either limited by the costs (in other word, you can make it, but it is to expensive to sell) and device physic limitations. After all, a conventional **MOS** transistor needs at least a few doping atoms in its source and drain region and since the density of doping atoms must be considerably smaller than the density of **Si** atoms, you cannot make the transistor components arbitrarily small.
- What "economic limitations" mean is illustrated in the next picture



  - Here the costs of chip development is plotted (circles) and from the extrapolation of the resulting rather straight line predicted for the coming years (squares) and compared to the gross national product (***GNP***) of sizeable countries
  - The problem will be to recover these costs at roughly the same prize per chip. It means that you have to sell at lot more chips at each generation. Assuming that the capacity in memory chips increases fourfold every three years, the market for bits then has to grow much faster than about **60%** a year!