

## Exercise 4.4-1

### All Quick Questions to

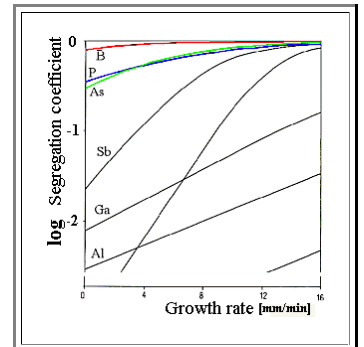
#### 4. Getting Started

##### Subchapter 4.1: Input to Si Processing in an Industrial Environment

- List (and discuss briefly) some essential inputs to a chip factory.
- What is the essential process for producing raw (= metallurgical) **Si** and what is the major use for this **Si**?
- Go through the essential of **Si** single crystal growth by the **CZ** technique. Give numbers and discuss in-situ doping, keeping the crystal dislocations-free, and any remaining problems.
- Describe shortly the essentials of how to obtain clean, doped poly-**Si** as needed for single crystal growth
- Where and why is a **CVD** process involved in making electronic grade **Si**?
- Describe the phenomenon of segregation. How does it impact **Si** crystal growth?

- Given the diagram on the right, discuss:

- What a segregation coefficient of , e.g.,  $10^{-2}$  means in terms of the concentration in the crystal in the beginning and the end of the crystal growth process if the initial concentration in the melt is  $10^{-6}$
- Why you prefer **As** to **Sb** as a dopant during crystal growth .



- Why is extreme flatness an essential condition for standard **Si** wafers?
- Why is it possible to keep wafers completely free of dislocations, but not of "microdefects" = agglomerates of point defects?

##### Subchapter 4.2: Other Semiconductor Growth Technologies

- Describe some problems encountered (and the solutions) when growing **III-V** single crystals.
- What are the incentives for trying to get **SiC** "to work"? Describe the specific problems encountered when growing **SiC** single crystals.
- Provide and describe major products not based on single crystal semiconductors.
- Explain the following abbreviations and give possible uses: **a-Si:H**, **μc-Si:H**, **CIGS**.

##### Subchapter 4.3: Infrastructure

- "Cleanroom class **100**" means roughly....?
- Describe the effects of *particles* on, and *contamination* in the chip.
- The electrically crucial area of an integrated transistor is **(50 × 300 × 300) nm<sup>3</sup>**. The lattice constant of **Si** is roughly **0.5 nm**; there are .... atoms per elementary cell. An **Au** concentration of **1 ppb** "kills" the transistor. How many Au atoms can you tolerate in your transistor? If you touch a gold ring and **1** out of **1 billion** surface atoms gets stuck on your finger - how many roughly are now on your skin?