9. Compound Semiconductor Technology

9.1 General Remarks

9.1.1 Major Differences to Silicon Technology

General Remarks

- In this lecture course it is assumed that you are tolerably familiar with main stream **Si** technology.
  - If you are not really acquainted with that subject, or you forgot most or parts of it, turn to the "**Electronic Materials Hyperscript**", specifically to chapter 4 and chapter 5.
  - We will not cover any part of compound semiconductor technology that is essentially identical to **Si** technology. This includes in particular lithography, ion-implantation, basic chemical vapor deposition, sputtering techniques, or basic plasma etching.
  - Instead we will focus on problems and solutions that are unique to the non-**Si** world. Of course, the backbone part will only contain a rather superficial glance on this subject - the details fill not only libraries but are developing at a fast pace.
- In this subchapter we will try to get a rough overview of the more general properties of compound semiconductors that we have to deal with.

Starting Material

- Huge **Si** crystals with diameters of **400 mm** weighing up to **250 kg** can be routinely grown - absolutely free of "large" defects like dislocations or precipitates, *and* with impurity levels in the low ***ppt*** (= parts per trillion) range.
  - This feat is simply not possible for compound semiconductors. This is not for lack of trying, but for *basic* thermodynamic and mechanical reasons - and this means that this deplorable state of affairs is not going away with more research and experience.
  - While the **GaAs**, **GaAlAs**, **GaP**, **InP**, ... (and so on) crystals will certainly become increasingly better with more and more applications (and thus money for crystal growth research and development), we may safely assume that no compound semiconductor crystal will ever get close in quality to a **Si** crystal. This sad fact, of course, limits some applications, while others are less affected.
- To understand the basic limitations, lets consider the growth of a **GaAs** crystal. Most problems are typical for its relatives, too.
  - We cannot just melt some **GaAs** and do some crystal pulling. As has a very high vapor pressure at the melting temperature (**1238 ^{o}C**) and would just evaporate off, leaving a **Ga** rich melt. And a **Ga** rich melt solidifies not far from room temperature into **GaAs** and **Ga** - until then it consists of *solid* **GaAs** with *liquid* **Ga** inclusions).
  - It is even worse for **GaP** or **GaN**. Whatever you do for crystal production, you must do it in a *high pressure* environment to keep the group **V** elements in the system.
  - Next, the **III-Vs** are generally much "softer" than **Si**, i.e. the have a smaller yield point. Compared to **Si**, small mechanical stresses are enough to cause plastic deformation - even at low temperatures. Since thermal gradients are *always* linked to mechanical stress *and* absolutely unavoidable during any kind of crystal growth, it is much harder to avoid dislocations in **III-Vs** than it is in **Si**. In fact - *it is impossible*.
  - Finally, any deviation from perfect stoichiometry must result in defects by necessity - the surplus atoms of whatever kind are included as point defects, agglomerates or precipitates. Compared to **Si**, where the density of intrinsic point defects is below $\mathbf{10^{-6}}$ even close to the melting point, you would have to have the mixture of the two elements precisely at $\mathbf{(1 : 1) +/- 10^{-6}}$ to achieve comparable point defect levels.
- Still, you can buy **GaAs** wafers with diameters of **150 mm** and dislocation densities below about $\mathbf{10^3\ cm^{-2}}$, a remarkable achievement of the material scientists involved. How this is done will be described in subchapter 9.2.2

Oxides

- **Si** microelectronics owes as much to **SiO_2** than to perfect **Si** crystals.
  - Not only is **SiO_2** a near perfect dielectric for many applications (its dielectric constant is large enough to make **MOS** transistors and capacitors efficient, but not so large as to produce large signal delays because of parasitic capacitors; its break-through field strength is among the highest measured; it is chemically extremely resistant yet easily etched in special chemicals and in plasma, and its interface properties are exceedingly good), but it can be produced in extremely good quality simply by thermally oxidizing the **Si**.
  - For compound semiconductors, however, we have a simple rule: *Forget about **III-V** oxides*
  - They are neither "good" (they may dissolve in water), nor can they be produced by oxidizing the crystal (there are always exceptions, of course).
- This doesn't make compound semiconductor technology easier! While there are many ways to get around this problem, it still is a problem.

Doping

- Semiconductor technology depends on being able to dope the crystal *both ways*: **p**-type conductivity and **n**-type conductivity is needed for most, if not all applications. Doping a semiconductor requires that *two* conditions are met:
  - *First*, dopants must exist - or more generally defects - that introduce electronic energy levels E_{dop} in the bandgap that are *very close* to the band edges. The difference in the energy levels, $E_C - E_{dop}$ and $E_{dop} - E_V$, must be comparable to **kT** (about **40 meV** at room temperature), otherwise the transfer of electrons between the bands and the dopant level does not occur at room temperature.
  - *Second*, the Fermi energy must be able to move freely - in must not be "pinned" by defect states. In other words, the energy states of the intentionally introduced dopants should be the only, or at least the dominating ones. If there are a lot of energy states stemming from defects like dislocations, precipitates, interfaces and so on, your Fermi level will be "pinned" to these states and doping is simply not possible or severely restricted.
  - In **Si**, this is not a problem. In many compound semiconductors, however there are big problems with this, especially for the **II-VI** compounds. As an example, it was the impossibility to produce ***p**-type doping* in *GaN* that prevented the use of this "blue" direct band gap material until recently.
- Doping thus is often a problem, and solving it in some hitherto unused semiconductor material is always a major break-through in materials science.

Contacts

- Any device needs at least two **ohmic contacts** for electrical communication with the "outside" world. An ohmic contact must meet two requirements:
  - Its ***I*(*U*)** characteristics must be linear for both polarities (This defines "ohmic").
  - The ohmic resistance, $\mathbf{d}U/\mathbf{d}I = U/I$, must be sufficiently low so that the voltage drop across the contact is negligible.
- Just putting some metal on a semiconductor does not necessarily produce a contact at all, you also must have some intimate interaction - usually you must heat the system somewhat. Otherwise you have a semiconductor - dirt/oxide - metal contact; mostly not what you want. Now consider the following list of **GaAs** features:
  - **GaAs** decomposes into **Ga** and **As_2**-gas at about **580 °C**.
  - The Schottky barrier height of **n-GaAs** is always large - about **0,8 eV** for any metal.
  - It is difficult to dope **n-GaAs** to a carrier concentration **$> 5 \cdot 10^{18}$ cm^{-3}** (larger concentrations would bring down the Schottky barrier height).
  - Annealing at temperatures up to **850 °C** for **30 min** is needed to activate implanted dopants.
- Put together, the list essentially says that there are no good ohmic contacts to **n-GaAs**. Still, we have working devices, so compromise must be possible. But metallization is a big issue for many compound semiconductors.