



Investor Information

[Overview](#)

[Board of Directors and Senior Management](#)

[Stock Quote](#)

[Stock Chart](#)

[Financial Reports](#)

[Financial History](#)

[Stock Trading Statistics](#)

[SEC Filings](#)

[Recent Press Releases](#)

[Archived Press Releases](#)

[Presentations](#)

[Audio Archives](#)

[Brokerage Firm Equity Research Analysts](#)

[Consensus Brokerage Research Analyst Pro forma Earnings Estimates](#)

[Calendar](#)

[Info Request](#)

[Dividend History/Stock Splits](#)

[Mail Alert](#)

[Stock Purchase](#)

Motorola Creates Revolutionary Semiconductor Materials; Potential to Transform Economics of Communications and Semiconductor Industries

SCHAUMBURG, Ill., Sept. 4 /PRNewswire/ -- Motorola, Inc. (NYSE: MOT) announced today that Motorola Labs scientists are the first to successfully combine the best properties of workhorse silicon technology with the speed and optical capabilities of high-performance compound semiconductors that are known as the III-V materials.

The discovery, which solves a problem that has been vexing the semiconductor industry for nearly 30 years, opens the door to significantly less expensive optical communications, high-frequency radio devices and high-speed microprocessor-based subsystems by potentially eliminating the current cost barriers holding back many advanced applications. For consumers, the technology should result in smarter electronic products that cost less, perform better and have exciting new features. The technology will change the economics and accelerate the development of new applications, such as broadband "fiber" cable to the home, streaming video to cell phones and automotive collision avoidance systems.

Other potential markets include data storage, lasers for such consumer products as DVD players, medical equipment, radar, automotive electronics, lighting, and photovoltaics. Until now, there has been no way to combine light-emitting semiconductors with silicon integrated circuits on a single chip, and the need to use discrete components has compromised the cost, size, speed and efficiency of high-speed communications equipment and devices.

Specifically, the discovery impacts the semiconductor industry by:

- Increasing substrate size, reducing substrate cost and processing costs for III-V manufacturing
- Integrating the superior electrical and optical performance of III-V semiconductors with mature silicon technology to create a new industry based on Integrated Semiconductor Circuits
- Extending the life of silicon and existing capital investments
- Improving cost effectiveness for higher performance applications such as optical communications
- Enabling larger scales of integration

"This is a tremendous achievement by our scientists and one that has the potential, when fully commercialized, to transform the industry in a way that is similar to the transition from discrete semiconductors to integrated circuits," said Dennis Roberson, senior vice president and chief technology officer, Motorola, Inc.

"Motorola's announcement that they have successfully made GaAs transistors in a thin layer of GaAs grown on a silicon wafer could go down in history as a major turning point for the semiconductor industry," said Steve Cullen, director & principal analyst, Semiconductor Research, Cahners In-Stat Group.

The Technology

The technology enables very thin layers of so-called III-V semiconductor materials (which include gallium arsenide, indium phosphide, gallium nitride and other high performance / light-emitting compounds) to be grown on a silicon substrate. Until now, this has been a virtually impossible task due to **fundamental material mis-match issues**.

Specifically, the underlying crystalline structures of silicon and the various III-V compounds do not match. As a result, previous industry attempts to combine them resulted in dislocations or "cracks" in the material as the two mismatched structures struggled to bond. The key to

solving the problem was **introducing an intermediate layer** of material between the silicon and the III-V material. The solution was found in discovering exactly the right "recipe" for a material that would easily bond with both silicon and GaAs, reducing the strain between the two target materials in the process.

The idea was originally developed by Motorola Labs' scientist, Dr. Jamal Ramdani. Developing and proving the exact recipe and process grew out of work done by a broad team of scientists and engineers. Motorola Labs is now working on developing the optimum intermediate layer for indium phosphide and other materials.

Another Industry First

Motorola Labs created the world's first 8" GaAs on silicon wafer and worked with epitaxial wafer manufacturer IQE to create the world's first 12-inch GaAs on silicon wafers and a variety of other wafer sizes. Motorola then made working power amplifiers from GaAs on silicon wafers and successfully completed numerous wireless calls using those devices in several phones over the past few months. In addition, a light-emitting device was created to demonstrate the optical characteristics.

"GaAs on silicon is just the first step and has created a baseline technology for extending our research to other materials systems," said Dr. Jim Prendergast, vice president and director, Motorola Labs, Physical Sciences Research Lab. "One of our next goals is to complete the task of growing indium phosphide on silicon. This technology should support chip clock speeds of more than 70GHz and long-wavelength lasers that are critical to fiber-optic communications."

Changing the Economics of Optical Communications

Until now, the industry has been dependent on costly gallium arsenide and indium phosphide wafers for optical and high performance applications. Because of their brittle nature, no one has previously been able to create commercial GaAs wafers larger than 6 inches or InP wafers larger than 4 inches. Scientists have also been unable to combine light-emitting semiconductors with silicon integrated circuits on a single chip.

"More than 90 percent of the existing fiber optic cable is still unused and underutilized," said Bob Merritt, vice president, Semico Research Corporation. "This technology could be the switch that eventually turns on those communications channels."

Plans to Commercialize

Motorola has filed more than 270 patents on inventions related to this new technology and the company intends to broadly license the technology. Padmasree Warrior, a Motorola corporate vice president has been selected to lead the commercialization effort. Warrior has worked in all aspects of the semiconductor segment, including device technology, research and development, process engineering, manufacturing and pilot line operations.

Technical Presentations

The technology breakthrough will be introduced to the scientific community at the following conferences:

Dr. Ravi Droopad, Principal Staff Scientist, Motorola Labs, will present at the International Workshop on Device Technology in Porto Alegre, Brazil, on September 4, 2001.

William Ooms, Director of Materials, Device, and Energy Research within Motorola Labs will present at the Materials Research Society Workshop in Chattanooga, Tennessee on September 11, 2001.

About Motorola

Motorola, Inc. (NYSE: MOT) is a global leader in providing integrated communications and embedded electronic solutions. Sales in 2000 were \$37.6 billion. Motorola Labs serves as the advanced research arm of the company, focusing on leading edge technologies for future products and product enhancements. Motorola also actively licenses technologies developed in the Labs to external customers.

Business Risks: Statements about the impact of this new technology are forward-looking and are based on current expectations that involve risk and uncertainties. Factors that could

cause actual results to differ materially from those in the forward-looking statements include: market acceptance of the technology; success in extending the technology to other materials; unanticipated technological delays; competing technologies; the cost of manufacturing the technology; and other factors found in Motorola's filings with the Securities and Exchange Commission.

Photos, artwork, b-roll and additional background material is available at the Motorola Media Center at: <http://www.motorola.com/mediacenter/> SOURCE Motorola, Inc.

CONTACT: Anne Stuessy of Motorola, +1-847-538-6192, or anne.stuessy@motorola.com; or Amy Smolensky of Hill and Knowlton, +1-312-475-5985, or asmolens@hillandknowlton.com, for Motorola/

Got it? Well, take it as an example of saying much without releasing any real information. Here is the real story from the ***Semiconductor International, 10/1/2001***

GaAs-on-Silicon, Finally!

Peter Singer, Editor-in-Chief -- *Semiconductor International*, 10/1/2001

Up until the late 1980s, GaAs-on-silicon was the focus of some intensive research at universities, wafer suppliers, MOCVD companies and research labs of many IC suppliers. The hope was that it would provide a platform whereby III-V optical devices and silicon digital technology could be combined on the same chip. But it really never proved viable, due to problems with the mismatch between the silicon and GaAs crystalline lattice, which caused a significant number of dislocation defects at the interface of the two materials, extending into the active area of the devices.

Suddenly, those problems appear to have been solved thanks to new research at [Motorola](#) (Schaumburg, Ill.). While working with **strontium titanate**, a material with a high dielectric constant (high k) that has applications as a gate dielectric and for DRAM capacitors, researchers noted that the lattice size of the material was such that it might make a good buffer material. "It turns out that strontium titanate has a lattice which is about 2% mismatched to silicon, but it's about halfway between silicon and gallium arsenide," said Jim Prendergast, vice president and director, Motorola Labs, Physical Sciences Research Lab. "The other interesting fact that we found out when we're growing this crystalline strontium titanate on silicon was that we're also getting ***an interface layer between the STO and the silicon, which was an amorphous silicon dioxide.***

Interesting! Epitaxial growth despite an amorphous layer between substrate and film. Has been observed before, however: I recount a paper growing something epitaxially on SiC with an amorphous layer between substrate and film, too. (around 1984)

"Amorphous silicon dioxide can act as a **compliant layer**. We believe that there is some level of compliance here. In fact, when we looked at the crystalline structure of the strontium titanate, it was completely relaxed. Based on that, one of our researchers, Dr. Jamal Ramdani, had the excellent idea of growing additional layers on top of the strontium titanate. His first try was to look at GaAs. He knew the lattice match would be pretty good to strontium titanate and, in fact, the second time he attempted to grow it, it was indeed successful." That was a little less than two years ago.

In other words: This was another one of the not-looked-for major discoveries!

"We've had just a crash program now here in Motorola Labs where we've been perfecting that technology, and we believe that we're at a point where we do have very good defect densities and are actually showing rf performance that's essentially equivalent to GaAs-on-GaAs," Prendergast added. Motorola Labs is now working on developing the optimum intermediate layer for indium phosphide and other materials.

Until now, the industry has been dependent on costly GaAs and InP wafers for optical and high-performance applications. Because of their brittle nature, no one has previously been able to create commercial GaAs wafers larger than 6 in. or InP wafers larger than 4 in. "We believe that GaAs-on-silicon starting material will be a lot less expensive than the equivalent GaAs-on-GaAs, even for the same wafer size," Prendergast said. "So a 6 in. GaAs-on-silicon would be significantly lower in production costs than an equivalent 6 in. GaAs-on-GaAs. You can imagine there would be even greater cost advantages in going to 8 in. or even 12 in." Motorola Labs created the world's first 8 in. GaAs-on-silicon wafer and worked with epitaxial wafer manufacturer IQE to create the world's first 12 in. GaAs-on-silicon wafers and a variety of other wafer sizes.

Motorola's announcement that it has successfully made GaAs transistors in a thin layer of GaAs grown on a silicon

wafer could go down in history as a major turning point for the semiconductor industry, said Steve Cullen, director and principal analyst, semiconductor research, [Cahners In-Stat Group](#) .

© Copyright 1994-2001 motorola, Inc. All Rights Reserved.

[Home](#) | [Terms of Use](#) | [Privacy Practices](#) | [Contact Us](#)