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Si/Al_2O_3/ZnO:Al capacitor arrays formed in electrochemically etched porous Si by atomic layer deposition

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Abstract

High surface area Si/Al_2O_3/ZnO:Al capacitors were formed in electrochemically etched porous silicon. The Al_2O_3 dielectric and the ZnO:Al top electrode were deposited by atomic layer deposition in high aspect ratio porous Si. A single capacitor with a typical area of about 1 mm^2 consisted of about 10^5 pores. Effective capacitance densities were between 2.0 and 2.5 $\mu F/cm^2$, i.e., approximately 30 times higher than for a planar capacitor prepared under identical conditions, illustrating the effect of the enhanced surface area in the porous structure.

Keywords: Macroporous silicon; Electrochemical etching; Atomic layer deposition; Thin films; High aspect ratio capacitor

1. Introduction

The number of passive components (inductors, resistors and capacitors) on a circuit board exceeds the number of integrated circuits in almost any application [1]. Because passive components occupy a large share of the space on a circuit board, miniaturization has been looked for. This is especially important in wireless products with increasing performance and functionality, where the share of passive components is highest. On the other hand, the minimum allowable size of a passive component is determined by the ability to handle and assemble the components on the board [2]. Traditionally, passive components have been discrete, i.e., single inductors, resistors and capacitors in their individual packages attached on the board with individual solder joints [1]. Research on integrating multiple passive components in a single package has been going on for some time, and various approaches have been studied [1,3]. One approach is to use thin-film deposition methods for the formation of several passive components on a single substrate (for example Si) [2,3]. These arrays or networks of passive components can then be packaged in single IC-like packages and attached on the circuit board [2]. In addition to saving space on the board, integrated passive components add to the reliability of the product since fewer solder joints are required [1].

High value capacitor arrays with capacitances from tens of nanofarads to several microfarads are needed as decoupling and energy storage capacitors [4]. In order to minimize the footprint area occupied by the capacitor array on the circuit board/package, capacitor designs with increased capacitance densities are required.

As seen from the well-known equation for a parallel plate capacitor (Eq. (1)), the capacitance density increases with decreasing insulator thickness, increasing insulator permittivity, and increasing effective surface area of the capacitor without increasing its footprint area

$$C = \varepsilon\varepsilon_0 A/t, \tag{1}$$

where C is the capacitance, ε is the relative permittivity of the insulator material, ε_0 is the permittivity of vacuum (8.85×10^{-12} F/m), A is the area of the capacitor, t is the thickness of the insulator. Commonly used insulator

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materials in thin film capacitors include SiO_2, Si_3N_4, Al_2O_3 and Ta_2O_5 [5–13].

When aiming to extremely high capacitance densities, it is necessary to combine the benefits achieved with a high permittivity insulator material and an increased effective surface area. With Si as the substrate material, the effective surface area can be increased by, for example, electrochemical etching that is a well-known method for the preparation of high aspect ratio structures in Si [14]. For example, electrochemical etching of moderately doped n-type Si under backside illumination in properly chosen conditions results in the formation of deep, straight, cylindrical macropores [14]. Electrochemically formed macroporous Si has in fact been used successfully for the preparation of high aspect ratio capacitors with layered $SiO_2/Si_3N_4/SiO_2$ insulators [11,12].

The increased surface area requires the ability to deposit thin films with conformal coverage and uniform film thickness on the walls of a high aspect ratio structure. For most thin film deposition methods this is extremely challenging, if not impossible.

Atomic layer deposition (ALD) is a chemical gas phase thin film deposition method that can be used for the deposition of metal oxides, nitrides and metals [15–17]. Because of its self-limiting growth mechanism, ALD is well suited for coating high aspect ratio structures such as deep pores and trenches. Film growth by ALD occurs via alternating saturative surface reactions. The precursor vapors are pulsed into the reactor one at a time, and the precursor pulses are separated by inert gas purges. After each precursor pulse and the subsequent purge, the substrate surface is saturated by a (sub)monolayer of that precursor. Since the gas phase is free of the first precursor, the next precursor reacts only with the adsorbed surface layer. Thus the film growth occurs (sub)monolayer by (sub)monolayer, and film thicknesses can be accurately controlled by the number of the deposition cycles. Films deposited by ALD exhibit excellent conformality and compositional uniformity over large and complex-shaped substrates.

Preliminary results on high aspect ratio capacitors with ALD-grown layered $Al_2O_3/Ta_2O_5/Al_2O_3$ and $Al_2O_3/HfO_2/Al_2O_3$ insulators were reported recently [13]. The porous Si substrates in that study were formed by dry etching.

This paper describes a simple, non-lithographic process for the preparation of high density $Si/Al_2O_3/ZnO:Al$ capacitor arrays by combining electrochemically formed high aspect ratio macroporous Si with atomic layer deposition of the insulator and the top electrode. Al_2O_3 was chosen as the insulator because of its relatively high permittivity and ZnO:Al as the top electrode material because of its easy etching.

2. Preparation of the n-Si/Al_2O_3/ZnO:Al capacitors

2.1. Preparation and properties of the porous Si

The macroporous Si was prepared by electrochemical etching. Pieces of n-type (100) Si with a resistivity of 1–4 Ω cm were used. In order to remove the native SiO_2 layer, the Si pieces were first dipped in 10 wt% aqueous HF solution for approximately 1 min. The electrical contact was subsequently formed by scratching the back surface of the Si piece, and rubbing some liquid In–Ga solder on the scratch.

The etching was done in a thermostated cell at 20 °C. Aqueous 4 wt% HF solution with a few drops of detergent was used as the electrolyte. Backside illumination was done using a LED array. The etch potential was 1.5 V, and the etch current density was decreased in a preprogrammed manner from the initial value of 8 mA/cm^2 to the final value of 7 mA/cm^2 during the etching. The etch current was controlled by adjusting the intensity of the illumination, i.e., the voltage used for driving the LED array [14,18]. The pores were formed by random nucleation, i.e., no initial pits were formed. The resulting pore diameters were approximately 2 μm, with similar pore wall thicknesses. Thus, about half of the surface was covered with pores. According to a simple calculation, the density of pores on the surface was about $1.6 \times 10^7/cm^2$. The etch duration was usually 100 min which resulted in a porous layer with a depth of 50 μm. Thus the aspect ratio of the structure was about 25 and the enhancement of the surface area caused by the porous structure was about 50-fold.

2.2. Thin film deposition

Prior to the ALD growth, the porous Si substrate was dipped in aqueous 10 wt% HF solution in order to remove the native SiO_2 layer. The Si substrate was then rinsed with water and blown dry with N_2.

The capacitors were prepared by depositing approximately 50 nm of Al_2O_3 and 180 nm ZnO:Al by atomic layer deposition (ALD). The depositions were done at 250 °C in a flow-type F-120 ALD reactor (ASM Microchemistry Ltd, Finland) [19] that was operated under a pressure of about 10 mbar using N_2 as the carrier and purging gas. Trimethylaluminum (TMA), dimethylzinc (DMZ), and H_2O were used as the Al, Zn, and O precursors, respectively. The precursors were evaporated in their external reservoirs and led to the reactor through needle and solenoid valves. TMA and H_2O sources were kept at room temperature and DMZ at −20 °C. In order to ensure adequate diffusion of the precursor vapors and the gaseous byproducts in and out of the deep pores, prolonged pulse and purge times were used. The pulse times for TMA and H_2O were doubled and purge times tripled as compared to those normally used for flat substrates in this reactor. For DMZ, only the purge time was increased.

The Al_2O_3 film was deposited using precursor pulse lengths of 2 s and purge lengths of 3 s for both TMA and H_2O. The growth cycle was repeated 500 times. ALD of Al_2O_3 from TMA and H_2O is a well-known process and the excellent conformality of Al_2O_3 grown from $Al(CH_3)_3$ and H_2O has been demonstrated earlier [20,21].

The ZnO:Al films were deposited according to [22]. The DMZ pulse and purge lengths were 0.2 s and 2 s, respectively, and the H_2O pulse and purge lengths were 2 s and 3 s, respectively. 3% of the ZnO pulses were replaced by a sequence containing a 7 s purge, a 2 s TMA pulse, and a 10 s purge. The total pulsing sequence of 30 ZnO pulses + 1 TMA pulse was repeated 33 times. The resistivities of the ZnO:Al films were $5–10 \times 10^{-3}$ Ω cm, in agreement with those reported in the literature [22].

The film thicknesses were estimated afterwards from FESEM micrographs and were found to be in agreement with the deposition rates obtained on planar substrates.

2.3. Contact formation, device area definition and electrical measurements

The back contacts were made by evaporating an Al film (thickness about 75 nm) on the back side of the Si substrate, and by contacting a thin Cu wire to the Al film using In as a solder.

The front contacts were prepared by electron beam evaporation of Al dots (thickness about 75 nm) with 1 mm diameters on the ZnO:Al film. The device areas were defined by carefully etching the ZnO:Al film from the area between the dots with 2.5 M HCl. Using the above-mentioned etch technique, it is difficult to define the device area precisely, and thus the area may vary from device to device. Therefore the area of each dot was measured and estimated separately afterwards. The device areas were between about 0.7 and 1.33 mm^2. The capacitance–voltage curves were recorded with a HP4284A precision LCR meter using the parallel circuit mode. The ac voltage applied to the capacitor was 50 mV and the frequency of the ac signal was 10 kHz.

3. Results and discussion

Fig. 1 shows a cross-section view of the high aspect ratio capacitor structure and the corresponding elemental maps for Al, Zn and O. The elemental maps show that EDS signals from Al, Zn and O are detected from the entire depth (50 μm) of the porous Si layer. The inhomogeneity of the signals is due to partial peeling off of the films due to cross-section sample preparation by fracturing.

The secondary electron and backscattered electron images in Fig. 2 show details of the capacitor structure where all the layers are seen. The conformal growth of the amorphous Al_2O_3 and the polycrystalline ZnO:Al films along the pore walls from the top all the way to the bottom is clearly seen. The film thicknesses along the pores were found to be uniform. Thus it can be concluded that the pulse and purge times applied here were sufficiently long to produce uniform films conformally on the pore walls. Fig. 2 shows, however, "pits" in the ZnO film (maybe also in Al_2O_3) near the top of the porous layer. These pits were observed only near the top of the porous layer and are therefore suspected to result from the wet etching process that was used for the device area definition. With a better device area definition method this problem can naturally be avoided.

The effective capacitance densities measured from the high aspect ratio capacitors were between 2.0 and 2.5 μF/cm^2 (normalized to the footprint area). Fig. 3 shows an example of a capacitance–voltage plot of a high aspect

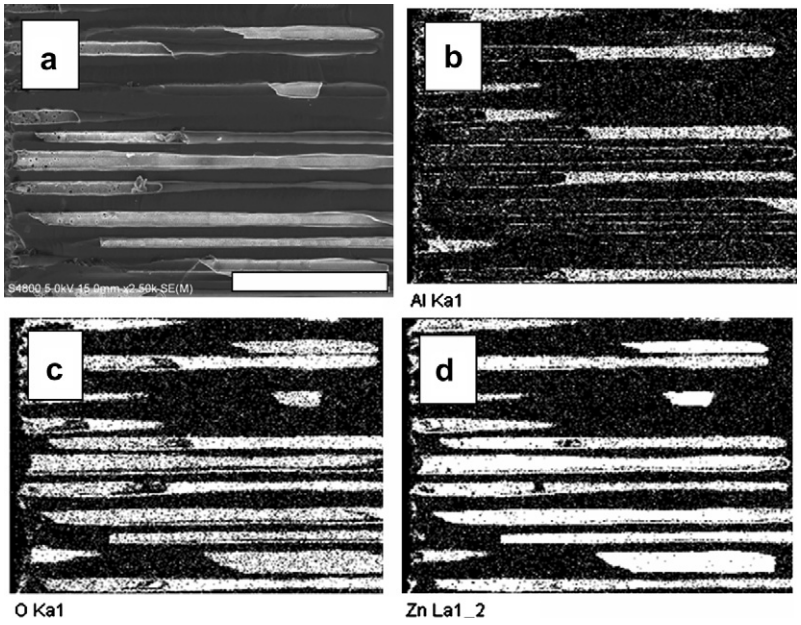

Fig. 1. (a) A cross-section FESEM image and corresponding elemental maps for, (b) Al, (c) O and (d) Zn. The elemental maps were acquired with an Oxford INCA Energy 350 energy dispersive X-ray spectrometer (EDS) connected with a Hitachi S-4800 field emission scanning electron microscope (FESEM). Scale bar = 20 μm.

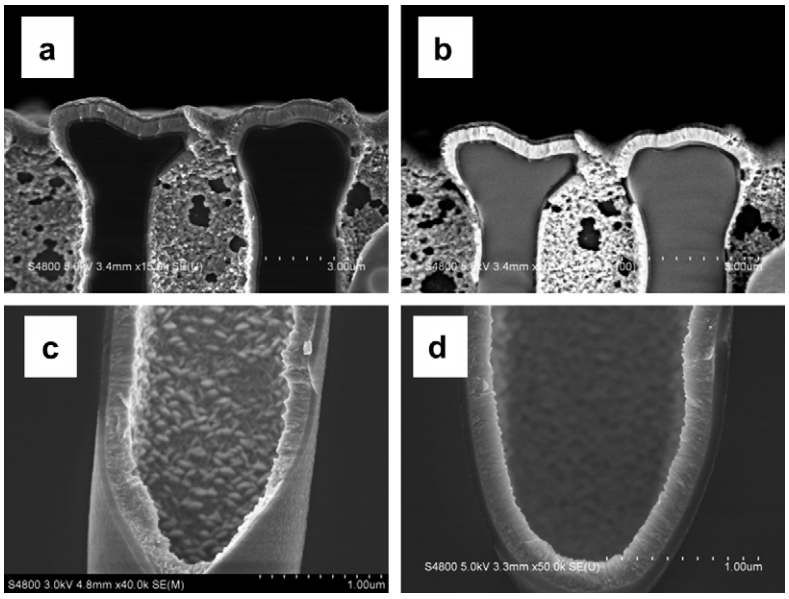

Fig. 2. Details from the top (a,b), middle (c) and from the bottom (d) imaged with secondary (a, c, d) and backscattered electrons (b). The images were acquired with a Hitachi S-4800 field emission scanning electron microscope (FESEM).

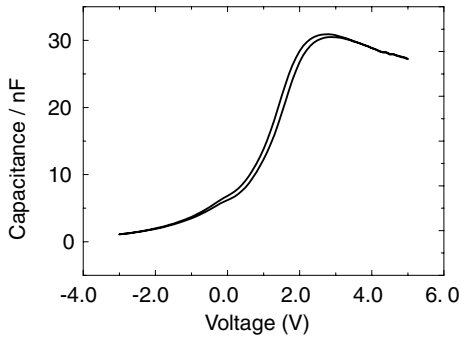

Fig. 3. Capacitance–voltage plot for a high aspect ratio $Si/Al_2O_3/ZnO:Al$ capacitor. Device footprint area was 1.33 mm^2.

ratio capacitor. The device with the highest capacitance density (2.5 $\mu F/cm^2$, or 25 $fF/\mu m^2$) had a footprint area of 1.33 mm^2 which corresponds to about 2.1×10^5 pores.

Both Lehmann et al. [11] and Roozeboom et al. [12] have reported ultra high aspect ratio MOS capacitors formed in electrochemically prepared macroporous Si. In both studies, the pore diameters were similar to those in this work, about 2 μm, but the pores were deeper, 150–165 μm, resulting in about a 100-fold surface area enhancement [11,12]. The insulator consisted of a layered $SiO_2/Si_3N_4/SiO_2$ (ONO) structure with a total thickness of about 30 nm [11,12]. The capacitors of Roozeboom et al. [12] showed effective capacitance densities of 10 $\mu F/cm^2$, i.e., about four times higher than those reported in this paper. Taking into account the different insulator thicknesses and permittivities, the lower capacitance densities observed in this work can be partly, but not completely, explained by the differences in the surface area enhancement factors. Based on the 50-fold surface area enhancement caused by the porous structure in this work, a 50-fold capacitance enhancement was expected as compared to planar capacitors prepared under identical conditions. The observed capacitance enhancement was only approximately 30-fold, however. This may indicate a parasitic capacitance in series with the device. The origin of this parasitic capacitance is most likely related to the Si substrate and/or to the ZnO:Al conductor. This idea is supported by the fact that the conductivity of the porous Si sidewalls in MOS capacitors is usually increased by phosphorus doping prior to the insulator formation [11–13]. Furthermore, phosphorus-doped polysilicon is commonly used as the top electrode [11–13]. Therefore, it seems likely that the lower than expected capacitances in this study are related to the unoptimal properties of the Si substrate. A third possible reason for the lower than expected performance is SiO_2 formation between the Si substrate and the Al_2O_3 film. On the other hand, a recent study [23] indicates that no interfacial SiO_2 formation should occur during the ALD growth of Al_2O_3 from TMA and H_2O.

Klootwijk et al. [13] reported capacitance densities of about 100 nF/mm^2 (10 $\mu F/cm^2$) for their high aspect ratio MOS capacitors. The porous Si substrate was prepared by dry etching. The porous layer was about 35 μm deep and had pore diameters of 1.5–2 μm and pore intervals of about 3 μm. The porous structure was reported to cause a 20-fold increase of the surface area. The insulators were three-layer structures of either $Al_2O_3/Ta_2O_5/Al_2O_3$ or $Al_2O_3/HfO_2/Al_2O_3$. This approach was considered to be beneficial in aiming to high capacitance densities together with minimal leakage currents. All insulator films were deposited by ALD and had thicknesses of 6–12 nm for Ta_2O_5, 5–10 nm for HfO_2 and 2–3 nm for Al_2O_3 [13]. Analogously to the results in the current study, the observed capacitance densities were 20–50% lower than expected. On the basis of TEM analysis, Klootwijk et al. [13] listed

several reasons for the unexpectedly low capacitance densities: roughness of the porous Si surface, variations in the thickness and crystallinity of the insulator films along the pore depth, and the presence of native SiO_2 [13].

In this work, the lowest leakage current at 5 V (which corresponds to an electric field of 1 MV/cm) was 1.6×10^{-4} A for a device with a footprint area of 1.13 mm^2. Thus the effective leakage current density is 1.4×10^{-2} A/cm^2 (normalized to the footprint area). Taking into account the 50-fold enhancement of the surface area caused by the porous structure, the "real area" leakage current density was 1.6×10^{-4} A $/(50\times1.13\ mm^2) = 2.8\times10^{-4}$ A/cm^2. On the other hand, as seen from Fig. 4, the leakage current was considerably lower at 2.5 V where the capacitance was at maximum. The leakage current at 2.5 V was only 1.7×10^{-5} A which corresponds to an effective leakage current density of 1.5×10^{-3} A/cm^2 and "real area" current density of 3.0×10^{-5} A/cm^2. Still, the leakage currents were considerably higher than those reported in the literature for ALD-grown Al_2O_3 on hydrogen-terminated Si [23]. For comparison, Klootwijk et al. [13] measured leakage currents of about 10^{-3} A/cm^2 at 1 V (presumably normalized to the footprint area) for their high aspect ratio capacitors with $Al_2O_3/Ta_2O_5/Al_2O_3$ insulator layers. Taking into account the 20-fold surface area enhancement by the porous structure, a simple calculation results in a "real area" current density of about 5×10^{-5} A/cm^2. The high aspect ratio Si/SiO_2/TaN capacitors of Black et al. [9] showed also similar effective leakage current densities as the capacitors in this work, about 10^{-3} A/cm^2 at 1 V. On the other hand, the leakage currents reported by Lehmann et al. [11] for their high aspect ratio capacitors with layered $SiO_2/Si_3N_4/SiO_2$ insulators were several orders of magnitude lower than those measured in this work.

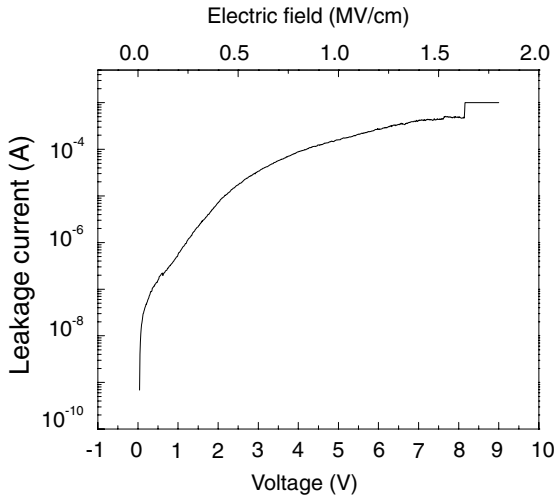

Fig. 4. Leakage current in accumulation as a function of applied voltage for a high aspect ratio Si/Al_2O_3/ZnO:Al capacitor. Device footprint area was 1.13 mm^2.

The high leakage currents observed in this work may be somehow related to the ZnO:Al conductor. It is possible that the wet etching process may have damaged also the Al_2O_3 layer. The pits in the ZnO:Al layer are clearly visible in the FESEM micrographs (see Fig. 2) but it is difficult to say if the damage goes all the way to the Al_2O_3 layer or not. The idea of ZnO:Al-related problem is further supported by the fact that also the planar devices prepared in this work under identical conditions showed high leakage currents. On the other hand it must be noted that the leakage current requirements for decoupling capacitors are not as strict as for some other applications [4,24]; according to [24], the leakage current of a decoupling capacitor is acceptable if its magnitude is considerably below the total current required by the IC.

Combination of ALD with electrochemically prepared macroporous Si offers several advantages for the preparation of capacitor arrays: a wide selection of materials can be deposited conformally with very accurate composition and thickness control. Moreover, capacitor arrays with different values can be achieved relatively easily by combining porous and flat areas, and by patterning the top electrodes with features of varying sizes.

4. Conclusions

A simple, non-lithographic process was developed for the preparation of high value capacitor arrays in electrochemically formed macroporous Si. High aspect ratio Si/Al_2O_3/ZnO:Al capacitors were prepared by atomic layer deposition of the insulator and the top electrode in the macroporous Si. The high surface area as compared to the footprint area resulted in capacitance densities between about 20 and 25 fF/μm^2. Leakage currents were high, however, which may result from unoptimal wet etching process used for the device area definition. Better results are to be expected by optimizing the device area definition process, thus resulting in lower leakage currents. The wide selection of insulator and conductor materials available by ALD allows the preparation of a variety of capacitor arrays with different values.

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