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Production and Investigation of Porous Si-Ge Structures for Thermoelectric Applications

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Mesoporous Si and Si-Ge are promising candidates for efficient thermoelectric converters needed for energy harvesting, e.g. from hot exhaust pipes of cars. Suitable mesoporous structures must meet a number of requirements concerning their geometry and processing costs, and suitable pore etching techniques have been developed. The paper addresses these issues, including the use of Si-Ge substrates from specially grown Si-Ge crystals. It is shown that most geometric and process requirements can be met by etching so-called current line pores under special conditions. First results concerning thermal and electrical properties are also presented.

Introduction

This paper focuses on producing porous Si (1 - 4) and porous Si-Ge layers with a geometry suitable for applications in thermoelectric devices. Thermoelectric devices can convert waste heat directly into electrical energy and have therefore considerable potential to lessen energy scarcity. Since they can provide electrical power independent of batteries or power circuits, they are also interesting for (mobile) sensor applications. The efficiency of a thermoelectric material is to first order proportional to the thermoelectric figure of merit *ZT*, which is given by

$$ZT = \frac{\sigma S^2 T}{\kappa}, \quad [1]$$

where σ and κ are the electrical and the thermal conductivity, respectively, *S* the Seebeck coefficient and *T* the absolute temperature. Thus a good thermoelectric material requires a high electrical conductivity but a low thermal conductivity, which is an oxymoron for bulk materials to some extend. However, because electrons and phonons have different mean free path lengths, it has been predicted that nanostructured materials can decrease thermal conductivity, while at the same maintaining a good electrical conductivity (5, 6). The validity of this concept has been shown for various materials (7, 8) and led to a renewed interest in thermoelectrics in the last two decades. It has been shown recently that this concept can also be applied to Si. While bulk Si is an inferior thermoelectric material, two publications showed that Si nanowires (SiNW) could have *ZT*s comparable to state-of-the-art materials (9, 10).

Nanostructured silicon is very interesting as thermoelectric material because it is relatively cheap and an extensive technological base is readily available. However, for mass-produced devices, macroscopic amounts of SiNW have to be produced and contacted (11), which complicates real applications considerably. Porous Si-Ge, i.e. Si crystals with a few percent of Ge, should even be better. Therefore we focused on porous Si and porous Si (3% Ge) as thermoelectric material. To some extent, porous Si is like an inverted

nanowires structure and therefore exhibits properties similar to Si nanowires. Compared to those, porous Si has the crucial advantage that it can be produced in macroscopic amounts at tolerable costs and that it can also be characterized much more straightforwardly. By varying wafer resistivities and electrochemical parameters, the structure geometry and thus the properties can be tuned.

Experimental Details

Proper mesoporous structures were etched using (100)-oriented n-type Si and n-(100) and n-(111)-oriented Si (3% Ge) samples with resistivity of (0.02 – 0.05) Ωcm or doping concentrations $N_D \approx 1 \cdot 10^{18}$ cm^{-3}. Etching has been carried out in the electrochemical cell described in detail in (12, 13) without illumination under (mostly) potentiostatic conditions. As electrolyte 48 wt. % HF dissolved in acetonitrile at a volume ratio of 1:2 was chosen for most of the experiments shown here because it gave the best results.

The Si-Ge samples were obtained by growing several (100) and (111) crystals with a Ge concentration of 3 wt.% and suitable doping levels in the $N_D \approx 1 \cdot 10^{18}$ cm^{-3} region, followed by cutting and polishing.

An FFT impedance spectrometer formed part of the etching system (ET&TE GmbH). The in-situ FFT impedance spectra were taken at intervals of 1 second in a frequency range between 20 Hz and 20 kHz, containing 27 frequencies.

Thermal and electrical properties were measured as function of temperature in a setup described elsewhere (14). Thermal conductivity measurements were performed by means of the 3-omega method (15). For measurement preparation a thin electrically insulating layer of spin-on-glass (IC1-200, Futurrex Inc.) was spin-coated on the samples. Using standard lithography and thermal evaporation a metal stripe was fabricated on top of the insulating layer. This metal stripe serves as heater and thermometer in the 3-omega measurement. From the frequency dependence of the measured temperature amplitude the thermal conductivity can be deduced (15).

Electrical conductivities of just etched and also re-doped porous membranes were determined by electrical van der Pauw measurements (16).

Pore Etching Results and Discussion

General Goal

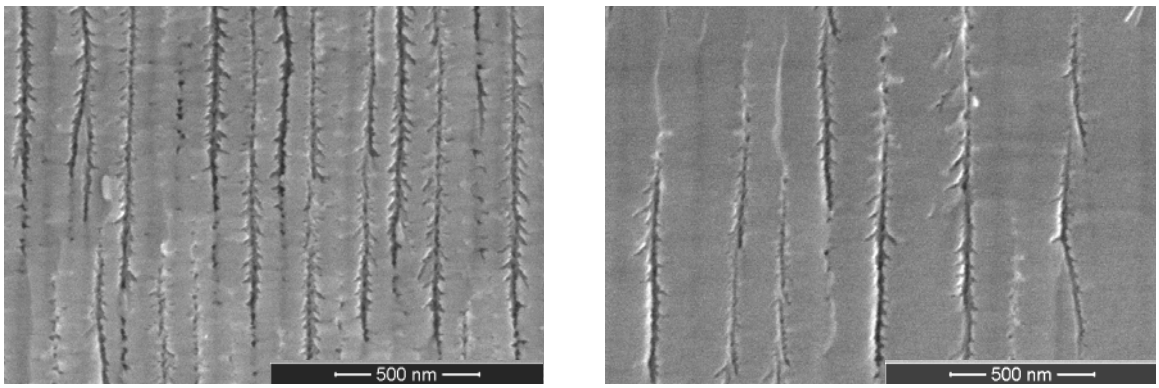
The first challenge lies in etching suitable pores rapidly, because of cost considerations, and with a defined and well-controlled geometry to relatively large depths of > 100 µm. The distance between pores, defining the “nanowire” size, should be in the 50 nm range, and the pore walls should be structurally as perfect as possible, for example not containing side pores, to minimize scattering of carriers and thus the resistivity. This requires so-called “current–line pores” which so far were mainly found in III-V semiconductors (17). Current line pores grow strictly in the direction of current flow in contrast to the more ubiquitous crystallographic pores extending in certain “easy” directions like <100> and <113> for Si. While many kinds of mesopores with suitable basic geometries have been etched before, see Refs. 18 - 22 and references therein, none of these prior experiments could meet the criteria given above. In particular, most mesopores produced so far are most likely of the crystallographic type and too heavily branched.

Another necessary task was to provide data about pore etching in Si (3% Ge) samples about which no prior knowledge existed. While one would not expect big differences to pore etching in pure Si, pore etching in pure Ge is known to be completely different from Si (23 - 25) and experimental work was needed to settle the issue.

In what follows we address results to some of the major points, omitting many details obtained from numerous experiments for the sake of brevity.

Pore Etching in Si (3% Ge)

The basic finding is simple and expected: there is no major difference in pore formation for Si and Si (3% Ge) if all other parameters are similar. The only difference found on occasion concerns only the surface pore density and uniformity as it can be seen in Fig. 1. The reason for this could be traced to the perfection of the surface polishing; commercial Si wafers are “better” than lab-polished Si(Ge) wafers.

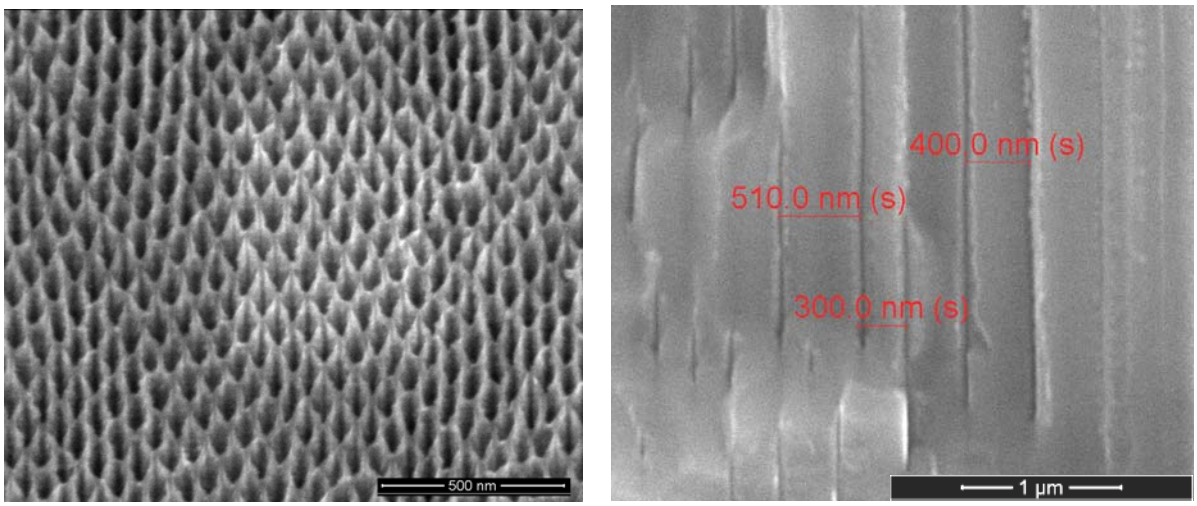


a) b)

Fig. 1 a) Mesopores in Si. b) Mesopores in Si (3% Ge), all other parameters being equal.

Pore Geometry and Conductivity

The average distance between the current line oriented (current-line) pores produced in this work and most likely also for the majority of crystalographically oriented mesopores (crysto mesopores) shown in the literatures strictly given by twice the width of the space charge region (SCR) and thus rigidly linked to doping and to the applied potential, as is seen in Fig. 2 and Fig. 5. This means that pore wall thicknesses in the desired range of 50 nm cannot be made with lightly doped Si, and many experiments proved that this undesirable but expected effect cannot be avoided. Since surface charges after etching still produce a SCR in the pore walls, the conductivity is not as good as it could be for flat-band conditions. The antidote to this effect consists of re-doping the Si after pore etching to higher doping levels, which is obviously more difficult to do if the doping level is already quite high. Anyway, in what follows we only consider doping levels of $N_D \approx 1 \cdot 10^{18}$ cm^{-3} that are in the targeted range for the pore wall dimension.



a) b)

Fig. 2 a) Mesopores in (0.005 - 0.02) Ωcm Si; top view. The pore wall thickness is about 40 nm. Note the formation of a self-organized mesopores in a). b) Mesopores in (0.1 – 1.0) Ωcm Si (cross section) with pore wall thickness around 400 nm.

Current Line Pores

The current line or "curro" pores as found most prominently in n-InP (26) would meet all of the requirements enumerated for Si / Si(Ge). The approach therefore is to emulate the conditions promoting the growth of similar pores in Si. Following the guidelines of the current burst model (4, 27) that have proved to be viable before (28, 29), electrolytes with small "oxidation power" were called for and after a series of tests with various "organic" electrolytes (13), 48 wt. % HF dissolved in acetonitrile in a volume ratio of 1:2 emerged as the best choice so far. Since in typical {100} samples current line pores and crystallographic pores both grow perpendicular to the surface in <100> direction, a number of indirect observations must serve to prove that the pores are current line, indeed.

First, the high growth rates of, that could be obtained, e.g. 7 µm/min, give a clear if indirect argument for current line pores since growth rates this large have never been demonstrated for crystallographic pores but are typical for curro pores. Next, the observation of self-induced diameter oscillations always accompanied by voltage oscillations under galvanostatic conditions (see Fig. 3) makes almost sure that the pores are current line in character. This effect so far was special to the curro pores in InP (30) that we try to emulate.

Just as telling are the in-situ FFT impedance spectra obtained. They can be fitted very well with the model used for curro pores in InP (see (31, 32) for details) and show identical behavior with respect to etching parameters. The pores shown in Fig. 4 and obtained with a {111} Si-Ge sample also prove the point. They grow perpendicular to the surface in a <111> direction, something never observed for crystallographic pores in Si. We thus can state with confidence that the mesopores in this work are current line pores.

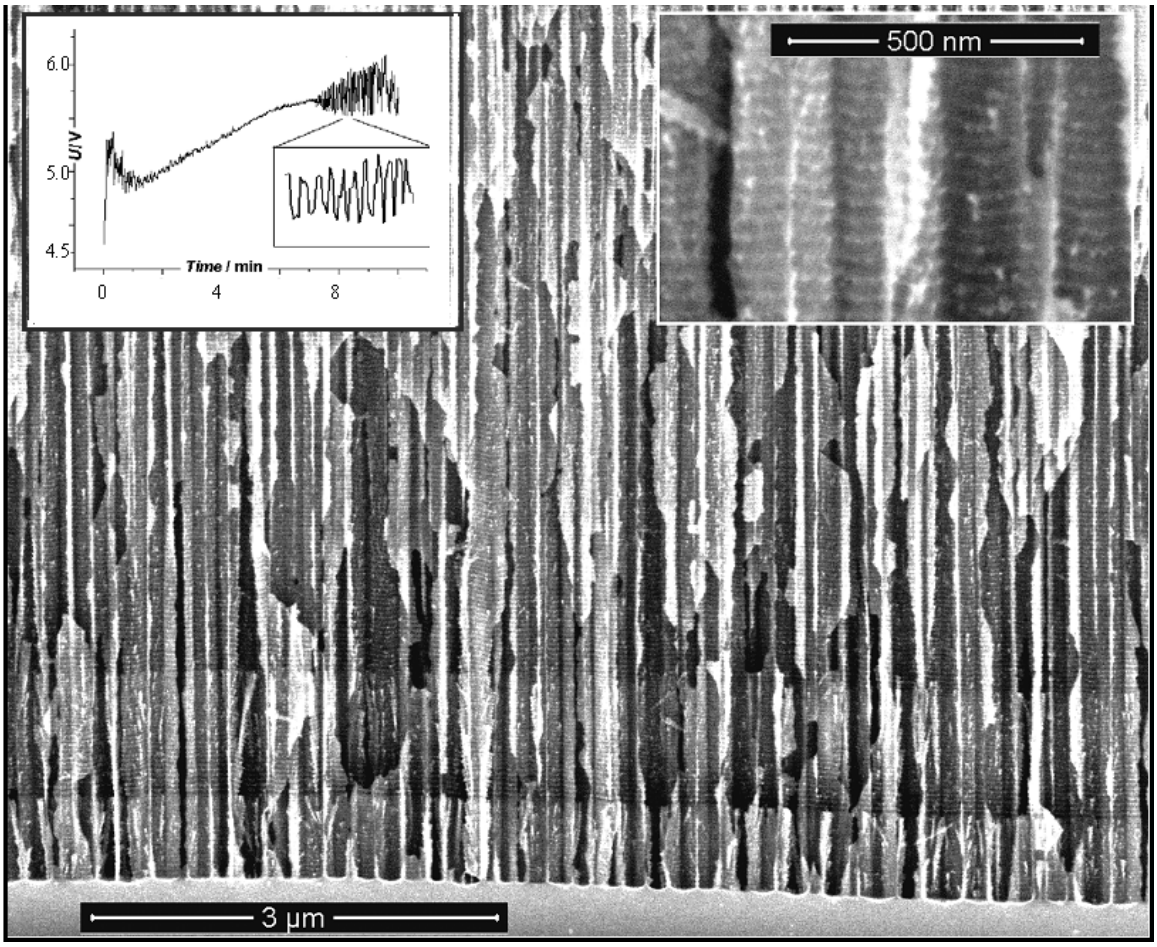


Fig. 3 Cross section of mesopores in (0.005 - 0.02) Ωcm Si with self-induced diameter oscillations. The insets show an enlarged view of the synchronized diameter oscillations and the concurrent voltage oscillations.

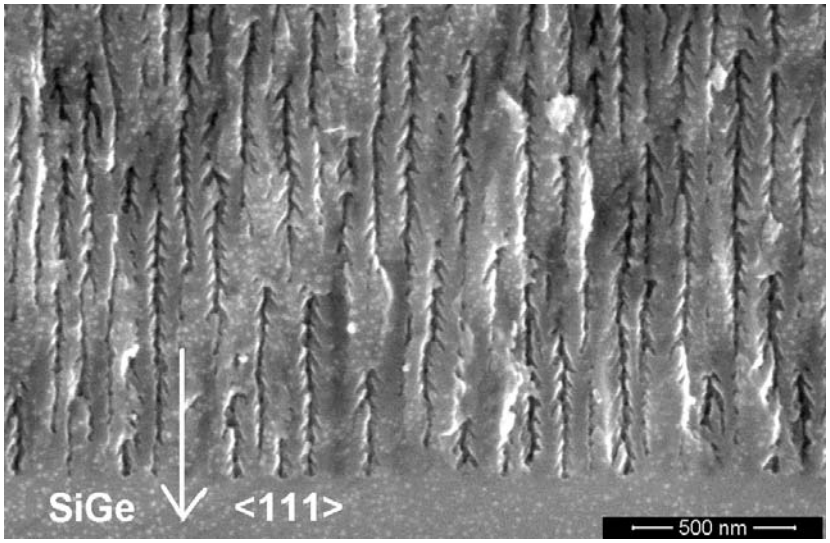


Fig. 4
Cross section of mesopores in (0.005 - 0.02) Ωcm (111) Si (3% Ge). The pores grow in <111> direction, which is not an "allowed" crysto-mesopore direction. The side pores, however, appear to grow preferentially in "allowed" <113> directions.

Structure Optimization

After the initially large parameter space could be narrowed down by the work related above, the major remaining task was to optimize the pore structures obtained so far. Depth uniformity, smoothness of pore walls, reduction of side pore formation, and better uniformity of pore nucleation on large areas, were and are the major issues to be addressed.

The available parameters for optimization are the applied external voltage, fine-tuning of the electrolyte, nucleation procedures, and the temperature. Here we report about the dependence of pore morphology on the applied external voltage and on some fine-tuning of the electrolyte. Fig. 5 shows effects of the applied potential. The external voltage has some influence on the pore wall thickness d_{PW} (it decreases with increasing the applied voltage as is to be expected from SCR considerations) but has no influence on the pore diameter $d_P \approx 30$ nm, which remains the same for all applied external voltages.

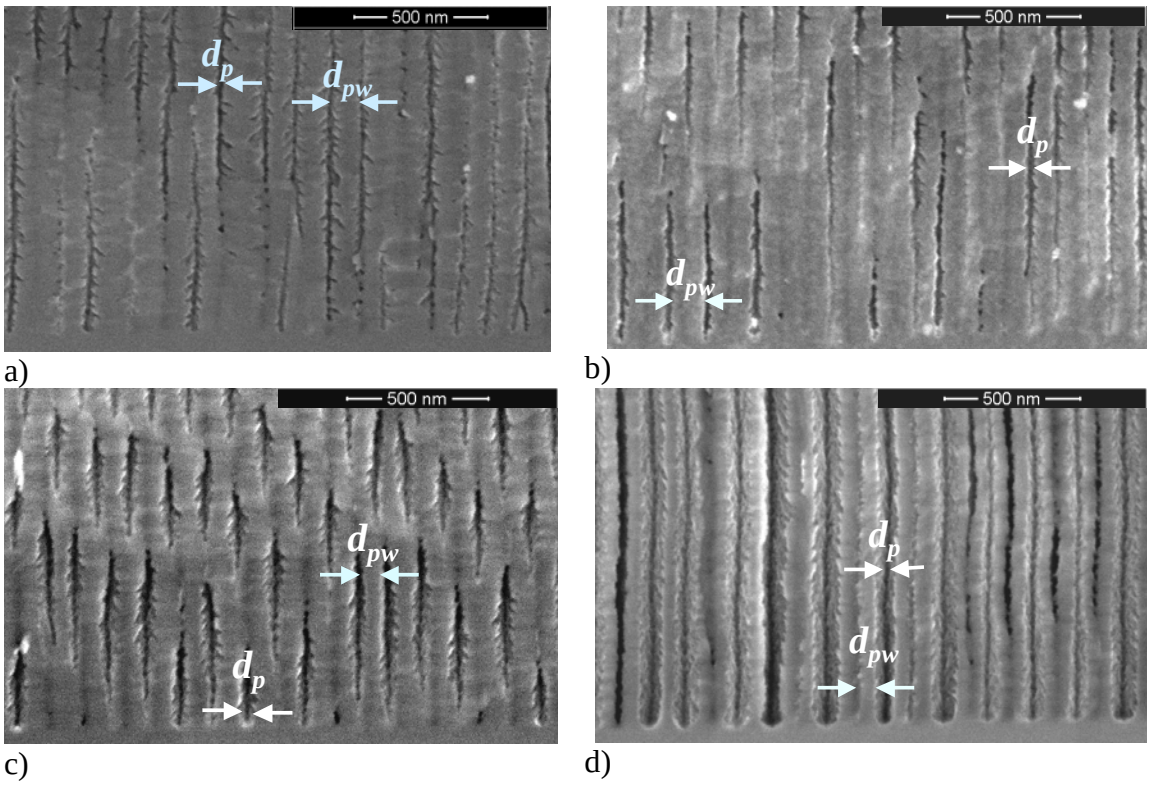
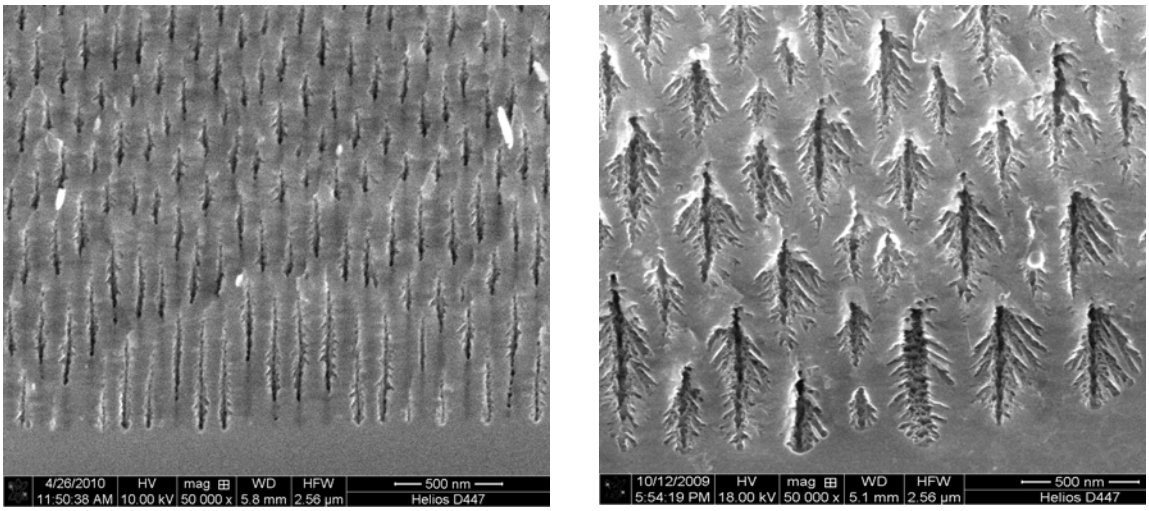


Fig. 5 Cross sections of the mesopore tip regions (d_P = pore diameter, d_{PW} = pore wall thickness, l_P = pore length, v = average growth rate). Parameters were: a) 0.5 V, l_P = 112 µm, v = 3.7 µm/min, b) 1 V; l_P = 135 µm, v = 4.5 µm/min; c) 2 V, l_P = 156 µm, v = 5.2 µm/min, and d) 5 V, l_P = 161 µm/min, v = 5.4 µm/min.
For all applied voltages the pore diameter d_P was nearly the same in the range of 30 nm. The thickness of the pore walls d_{PW} is smaller at higher applied voltage (e.g. $d_{PW} \approx$ 55 nm for 5 V) and is larger at lower applied voltage (e.g. $d_{PW} \approx$ 120 nm for 0.5V).

Side pore formation (and current and thus growth rate) increases with increasing voltage. In essence, small voltages are favourable from a pore morphology point of view, larger voltages from a growth rate point of view. Since the pore structure also changes as a

function of pore depth, a best compromise will be to run a $U(t)$ profile, with some feed back from the impedance measurements.

Only one observation with respect to electrolyte optimization will be reported here; the work on this topic is not yet finished. Acetonitrile as solvent for the HF is chosen because it minimizes the water content of the electrolyte and thus the "oxidation power" (33). To check if this reasoning was sound, some experiments were done with an acetonitrile : HF : H_2O electrolyte with typically 1:1:1 of water added. Fig. 6 shows a typical result.



a) b)

Fig. 6 a) Pore tips obtained with undiluted acetonitrile : HF = 1 : 1. b) Pore tips obtained with acetonitrile : HF : H_2O in proportion 1:1:1.

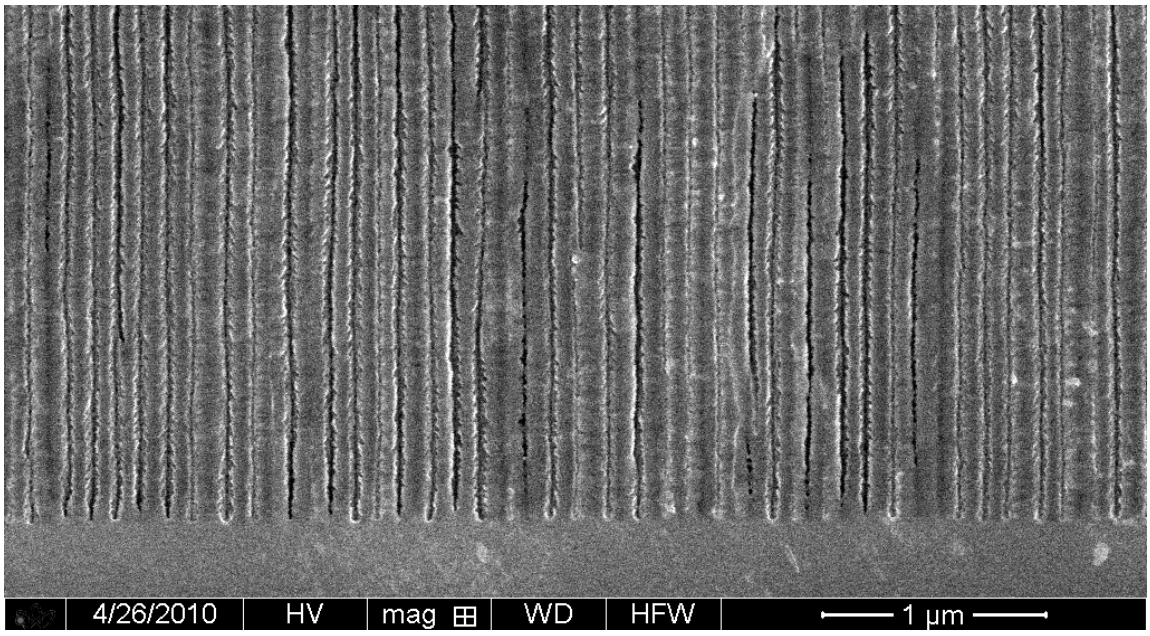


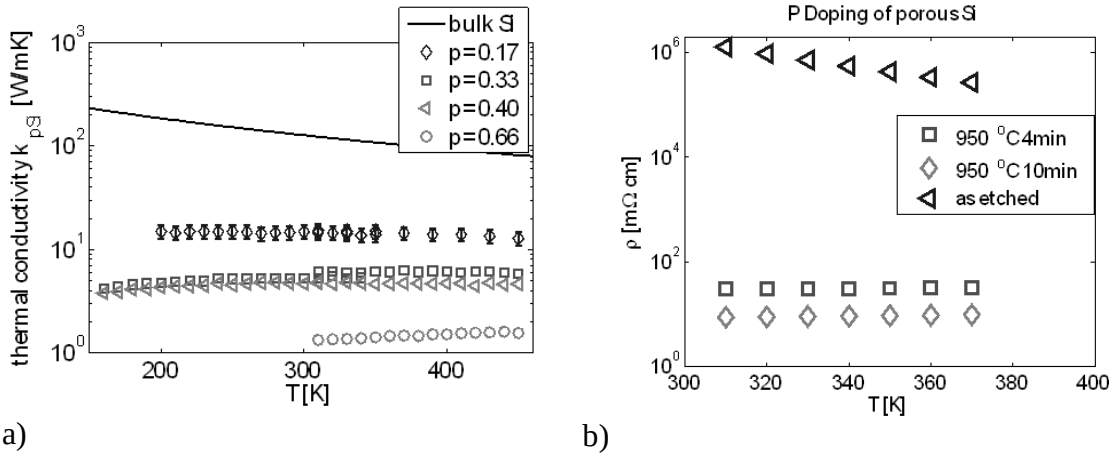
Fig. 7 „Best pores"; tip region. The pore wall thickness averages to d_{PW} = 100 nm, pore diameter is d_P = 30 nm, total pore length l_P = 135 µm. With an etching time of t_P = 30 min an average growth rate of v = 4.5 µm/min was achieved.

It is clear that water-free electrolytes as far as possible are best and that the basic reasoning concerning this point is sound. While many other electrolytes have been tried, too, further improvements are still possible. Lowering the temperature a few degrees or increasing the viscosity of the electrolyte has been shown to improve pore morphologies in other cases, for example (34, 35) and need yet to be tried. Fig. 7 shows the best pore structures produced so far. While not all goals are met yet, these pores already show promising electrical and thermal parameters.

Thermal and Electrical Measurements

The thermal conductivity was measured on bulk Si and Si-Ge and on samples with different pore geometries expressed summarily as porosity. Fig. 8a) shows results. Generally, the thermal conductivity is reduced at least one order of magnitude; for higher porosities a reduction of two orders of magnitude is possible. This is as expected in a previous work (36).

Measurements of the electrical resistivity showed that the porous layers had a rather high specific resistivity, decreasing with temperature as is typical for semiconductors. This was expected since much of the remaining Si is "filled" with SCR resulting from surface charges and thus an insulator. The antidote is increasing the doping level (called re-doping). This was done by a spin-on technique using a liquid dopant precursor for phosphorous (P) and boron (B), followed by annealing with parameters as shown in Fig. 8b). Shown are the results for P re-doping; the results for B are comparable. The resistivity could be decreased by 5 orders of magnitude and the temperature behavior now is reminiscent of semi-metals.



a) b)

Fig. 8 a) Thermal conductivity as a function of temperature *T* for bulk Si and samples with various porosities as indicated. b) Resistivity for etched porous samples and after re-doping with P. Doping time and temperature are given in the legend.

Conclusions and Outlook

The experimental evidence so far supports the claim that mesoporous Si could be an attractive material for thermoelectric applications. Porous structures with strongly decreased thermal conductivity can be produced with reasonable parameters for mass production. Re-doping can increase the poor electrical conductivity of freshly etched porous substrates and the figure of merit achievable is much higher than that for bulk Si.

Much work remains to be done, however. In particular the interplay of the fine structure of the porous layers and electrical conductivity need to be investigated and further optimization of the etching process is necessary.

Acknowledgements

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