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Development of three-dimensional microstructure processing using macroporous *n*-type silicon

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Abstract. The development of a micromachining technique for processing arbitrary structures with high aspect ratios in bulk silicon is presented. It is based on utilizing standard microelectronic processes and electrochemical macropore formation on *n*-type silicon in electrolytes containing hydrofluoric acid. This pore-etching technique allows us to produce very regular pore arrays with pore diameters and distances in the micrometer range and pore lengths up to wafer thickness. Samples with prefabricated pore arrays which differ in pore spacing, pore diameter and geometry are used as substrates for a micromachining process. The pores will facilitate the anisotropic etch profile which is required for the desired high aspect ratios although an isotropic etch process is used. Very deep microstructures with steep pore walls and aspect ratios of 10–15 are produced with this technique. It is shown that smaller pore array dimensions improve microstructure resolution.

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Micromechanics, and, as a logical result, microsystem technology, has been developed for the preparation of micrometer structures, pumps, tools, turbines and Microelectromechanical Systems (MEMS) like fully operating actuators and sensors [1, 2]. For example, promising applications are in optics, fluidics, biomedical and medicine techniques, and microscopy with Scanning Tunneling Microscopes (STM) or Atomic Force Microscopes (ATM) [3, 4]. However, microsystem technology is just at the beginning of its commercial development.

Micromechanics has evolved from silicon technology and therefore the commonly used techniques like alkaline etching, plasma etching and laser-induced processes are used for the realization of structures with small dimensions and high aspect ratios [1, 2, 5, 6]. In addition, the LIGA technique (lithography, electroplating, molding) has been established in the early eighties [7, 8]. Metallic, polymeric or ceramic microstructures are produced with this technique, which are subsequently used as molds for electroplating. The LIGA process requires X-ray mask fabrication, synchrotron radiation and X-ray-sensitive photoresists, in most cases polymethylmethacrylate (PMMA). The first two facilities are cost-intensive and generally not available in common laboratories. Recently, a low-cost alternative process which uses UV-sensitive polyimide photoresist is reported in [9]. However, both techniques cannot be applied for direct silicon micromachining. The technique of LIRIE reported in [10], which is a combination of approach of *li*thography and *r*eactive *i*on *e*tching, offers the possibility of directly processing silicon microstructures. However, this technique has the disadvantage of the formation of non-ideal steep sidewalls.

Since the discovery of the luminescent properties of microPorous Silicon (PS) in the beginning of this decade [11, 12], the main prospect for researchers in this field is integrating optical functions into silicon solid-state devices. This is reflected in over 1500 publications which have been published during the last five years. To our knowledge, the idea of using Porous Silicon Layers (PSL) in micromachining has so far only been reported in [13, 14]. The electrochemical macropore formation in electrolytes containing Hydrofluoric Acid (HF) on *n*-type silicon of (1 0 0) orientation, reported recently [15], is a micromechanical process itself and offers a multitude of possibilities for further development. The etching technique allows to produce pores with aspect ratios of up to 250 and a constant pore density. Recently, we have presented a new technique for direct silicon micromachining that combines the macropore etching and an isotropic plasma etch process and is fully compatible with standard microelectronic processes [16]. Using this technique we are able to produce microstructures with high aspect ratios up to 15 and steep sidewalls. However, some irregularities still remain at the sidewalls of the microstructures. In this paper, we report on the pore-etching process itself and microstructure resolution improvement by using different pore arrays concerning diameter, spacing and geometry.

1 Experimental

The electrochemical setup for the macropore etching is shown in Fig. 1 and is described in detail elsewhere [15, 17]. The starting material was *n*-type silicon (1 0 0) with different doping densities. An n^+-doped backside serves as an ohmic contact. Since holes are necessary for anodic silicon dissolution in HF, the backside of the sample was illuminated to increase the flux of minority carriers. An optical high-pass filter was used to prevent holes from penetrating into the pore walls. The frontside of the wafer was exposed to the electrolyte. Etch pits, which define the pore patterns described in a subsequent section and serve as nucleation centers for the pore growth, were obtained by standard lithography and subsequent alkaline etching.

All deposition and evaporation processes and photolithography are standard processes in microelectronics. The etching of the microstructures was carried out chemically in a Freon® 14 and oxygen (CF_4/O_2) containing plasma (600 W, 500 mT) in a BRANSON IPC Barrel reactor.

The current–voltage curve was recorded with a homemade potentiostat with a standard three-electrode arrangement which consists of a platinum (Pt) counter-electrode and a saturated calomel (SCE) reference electrode connected to the cell via an agar–agar bridge filled with potassium chloride (KCl).

2 Pore formation process

It is not the purpose of this paper to describe the phenomena related to the silicon/HF-electrolyte interface and the formation of porous silicon in detail. Therefore, only a summary containing the main topics of macropore formation is presented here. For particular information, the reader is referred to [18, 19] and the references therein.

It is well known that bulk silicon is electrochemically etched under anodic bias in solutions containing HF and that holes (h^+) are required for the creation of PS [20]. In general, the electrochemical reaction at the silicon electrode is limited either by charge transfer described by the Tafel law or by diffusion of reactive ions in the solution to the electrode surface. Both can be distinguished by different slopes in the current–voltage plot. As a consequence, there are two different regimes with a transition region in between where the *i–U* behavior changes from charge-supply-limited to diffusion-limited. This can be seen in the potentiostatic *i–U* curve of an illuminated *n*-type silicon sample in Fig. 2. The transition region is characterized by a specific current peak i_{PS}. For current densities below i_{PS}, porous silicon is formed because HF accumulates at the surface and every hole that reaches the surface is consumed resulting in silicon dissolution and pore formation. For current densities above i_{PS}, holes accumulate at the surface and HF is depleted. Consequently, hills on the surface are preferentially dissolved because the mass transport, which is lower in depressions or pits, is the rate-determining step, i.e. electropolishing occurs [21].

The formation of small, microporous structures (with dimensions < 2 nm, according to the IUPAC convention) in *p*-type silicon and highly doped *n*-type material is attributed to a self-adjusting phenomenon due to hole depletion of the pore walls by quantum confinement [11]. For larger structures: (*i*) > 2–50 nm (mesoporous) and (*ii*) > 50 nm (macroporous), this effect could be neglected and another mechanism must be responsible for pore formation.

Recently, we have shown that the meso- and macropore formation in low-doped *n*-type Si can be also explained by a self-adjusting process with the main topic being the steady-state condition between ionic diffusion in the electrolyte and charge supply from the bulk electrode at the pore tip [15]. During the anodic dissolution, the characteristic critical current density i_{PS} is present at the pore tip, and the pore walls are depleted of holes due to the building of a space-charge layer. The latter determines the pore-formation process. Empirical equations were developed which enable us to regulate the diameter, spacing,

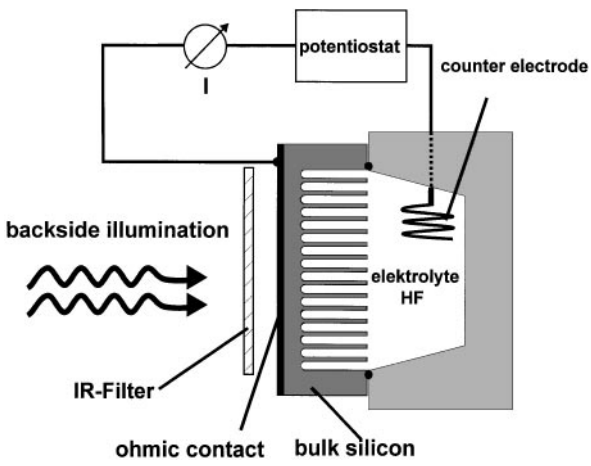

Fig. 1. The electrochemical setup for macropore etching

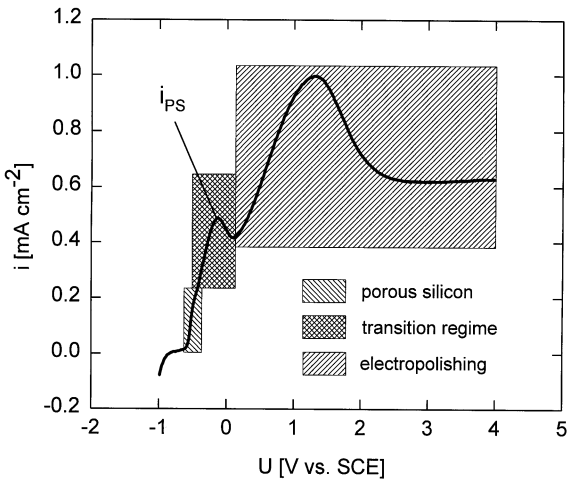

Fig. 2. Current–voltage curve for n-type silicon under illumination in 0.1 wt% HF. The three different regimes described in the text are marked by the striped areas

depth and growth rate of the pores, respectively, by adjusting the formation conditions like illumination, current density, electrolyte concentration and the substrate-doping density [15].

If the holes necessary for pore generation are supplied by backside illumination, nearly every hole is collected at the pore tip [17, 21]. Of course, the diffusion length of the minority carriers has to be comparable to the wafer thickness (several hundred μm). Using a defined pattern obtained by photolithography and subsequent alkaline etching, we are able to produce such regular pore arrays with aspect ratios of up to 250. The pore arrays in itself offer a multitude of possibilities for application in microtechnology in general. For instance, they were used in capacitor technology [22] and as photonic band gap material [23, 24].

It is important to note that the pore-formation process is limited to *n*-type silicon of (1 0 0) direction. In addition, the direct generation of microstructures by the pore-etch process is not possible because the generated porosity (etched volume/unetched volume) is always constant. The sample can only be homogeneously etched and the minimal scale for porosity variations is of the order of millimeters and determined by wafer thickness and minority carrier diffusion length, respectively. For direct generation of microstructures, variations in porosity of the order of micrometers are necessary.

3 The microstructure etching process

3.1 General concept

The general concept for the microstructure formation process is outlined in Fig. 3. It starts with macropore etching in bulk Si. The pores serve as a kind of "prepattern" for the microstructures which defined their depth and lead to the steep and straight walls. It is shown that the quality of the sidewall steepness and the resolution of the structures strongly depend on the choice of the pore array. The microstructures will be defined by a standard lithographic process. Subsequently, the depth-etching has to be performed. The pores, together with a sidewall passivation, will facilitate the anisotropic etch process which is required for the desired high aspect ratios. It is important to note that an anisotropic etch process is *not* necessary, but the anisotropy is forced by the pore array. Finally, after the removal of the mask, the pores will be filled to obtain a compact structure and better mechanical stability. A detailed description of the single-process steps is given in the following sections.

3.2 Pore arrays

We have used two pore arrays, which differ in pore diameter, spacing and geometry, to study effects on the performance of the etching process and the accuracy of the microstructures. Figure 4a and b show electrochemically etched arrays of macropores with an orthogonal (pore diameter, 2.00 μm; pore spacing, 3.5 μm; pore depth, 140 and 150 μm, determined array A in the following) and

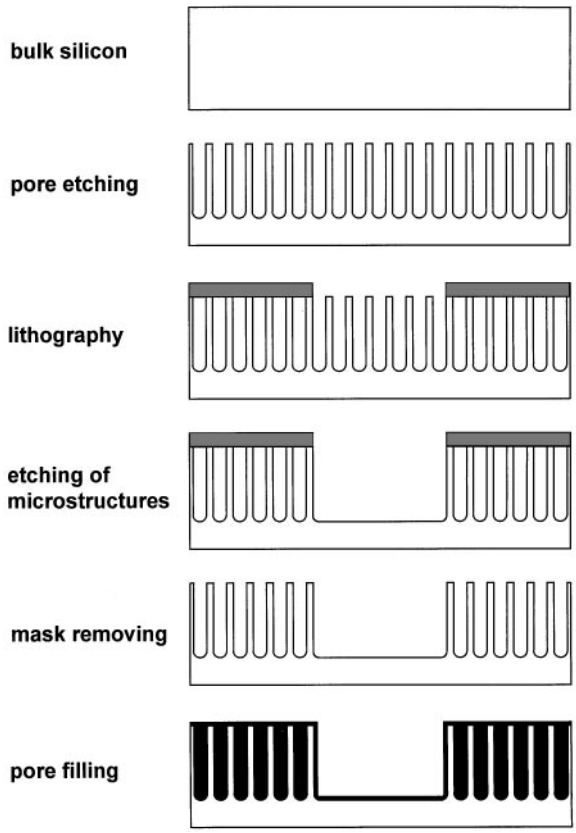

Fig. 3. General concept for the formation of silicon microstructures

a hexagonal pattern (pore diameter, 1.5 μm; pore spacing, 2.3 μm; pore depth, 80 and 75 μm, array B), respectively. It can be easily seen from the insets of Fig 4a and b that the hexagonal pattern shows a higher porosity (52.5% for array B in comparison with 36% for array A), which should shorten the depth-etching time and decrease the sidewalls roughness. In general, increase of porosity of the prepattern should improve the depth-etching conditions, because less bulk material has to be removed.

3.3 Sidewall passivation

The pores are used for the definition of the microstructure depth and the anisotropic etch process which results in high wall steepness. Therefore, it is desirable to raise the etch rate in the non-masked regime in comparison with the covered part of the sample. This is verified with an additional processing step, the passivation of the pore walls with a 100 nm Si_3N_4 layer. After the lithography and mask etching, the Si_3N_4 will be removed from the exposed regime with a wet chemical etch (see the next section). This will result in a higher microstructure etch rate for fluoride-containing etches in this regime in comparison with the mask covered part of the sample because the plasma etch rate for bulk silicon is much higher than it is for Si_3N_4 (selectivity: $\sim 5:1$). Some results that illustrate the passivation effect are shown in Fig. 7a and b in [16].

Experiments with other sidewall passivation layers, e.g. silicon dioxide (SiO_2), were also performed.

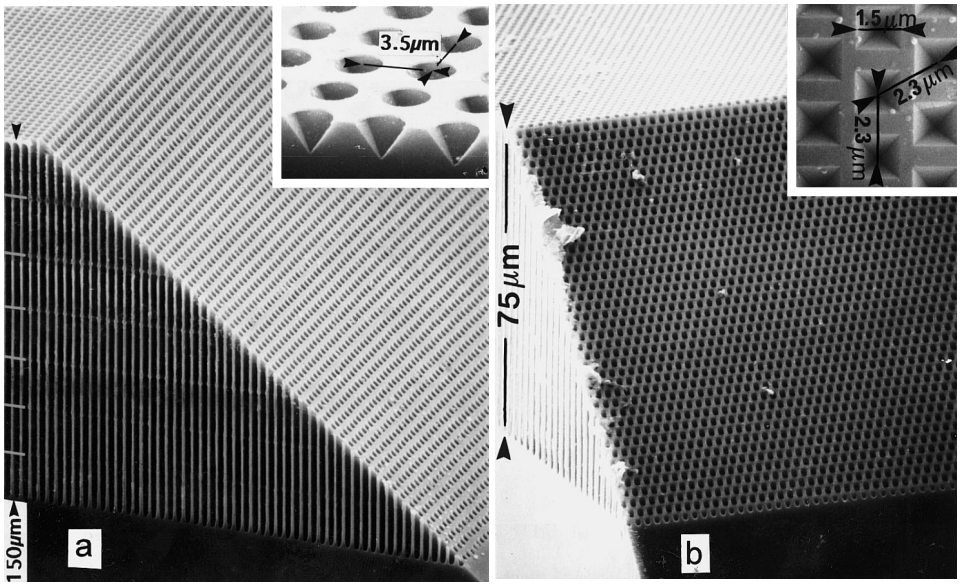

Fig. 4a, b. Surface, cross-section and a 45° bevel of n-type silicon samples showing the predetermined patterns of macropores: (**a**) orthogonal array A, (**b**) hexagonal array B. Pore growth was induced by regular patterns of etch pits produced by standard photolithography (shown on the upper right)

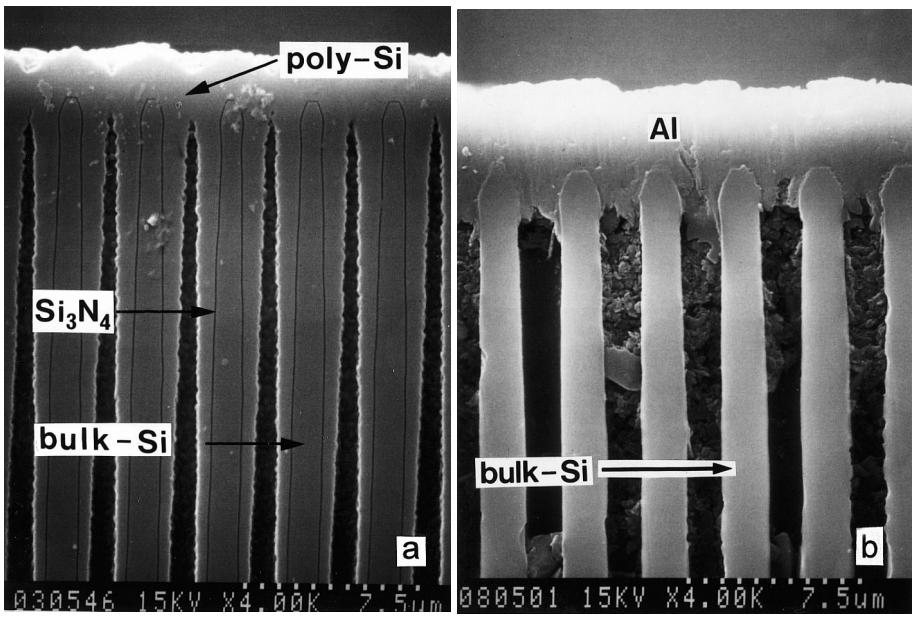

Fig. 5a, b. Two approaches for pore closing: (**a**) polysilicon deposition process obtained with high deposition rate (cross-sectional view); (**b**) Al evaporation (cross-sectional view) obtained after 3.5 μm evaporation of Al on pattern A

Unfortunately, thermal oxidation of the porous structures results in a very large wafer bow up to values of 2 mm for an oxide thickness of roughly 300 nm. Thus, it is very difficult to handle the wafers without introducing any stress-compensating process steps.

3.4 Mask technique and lithography

The surface of the sample is not flat but consists of a regular pattern of deep holes with thin walls in between. Therefore, lithography for the microstructures is rather complicated. Experiments were carried out with different photoresists which are directly coated on the substrate. The major problem of this technique is the loss of resist due to penetration into the pores and is described in [16].

Instead of directly coating the sample, it is necessary to close the pores. Two approaches were used: (i) polysilicon deposition and (ii) evaporation of aluminum [16], and the results are shown in Fig. 5a and b. A high polysilicon deposition rate will result in an increased polysilicon precipitation at the top of the pores. The pores will finally be closed before the deeper parts of the pores are completely filled, which, in general, allows the deposition of photoresist. The difficulties with this approach is with the microstructure etching process. From Fig. 5a one can imagine that during the deposition process the polysilicon is penetrating deeply into the pores (roughly 80 μm for a 120 μm deep pore). For the microstructure etching process it is desired to remove the wall passivating Si_3N_4 layer. The use of standard wet chemical etching techniques or plasma processes [25] for the removal of

polysilicon, that covers the Si_3N_4, probably destroys the photoresist layer and the mask, respectively.

Therefore, we decided to close the pores with Al which was evaporated on the top of the wafer. An example for a 3.5 μm evaporation of Al on pattern A is shown in Fig. 5b. It can be seen clearly that the pores are completely closed and that the Al is only deposited on top and in the first few micrometers of the pores. This mask is very stable and regular, although a certain roughness induced by the pore pattern remains. By using pattern B, evaporation of only 3 μm Al is sufficient because the pore diameter is smaller. The mask etching times are shortened and undercut problems are reduced.

For the transformation of the photolithography, a standard wet chemical, Al-etch-based, on phosphoric acid was used [25]. For the complete removal, the Al 3.5 μm thick mask of pattern A was etched for atleast 9 min and the resulting mask undercut is about 1–2 μm. The etching time could be reduced to 7 min for the 3 μm thick mask of pattern B. Here the mask undercut is below 1 μm. If anisotropic plasma etching for Al removal would be used, the photoresist mask undercut will be minimized, of course.

3.5 Removal of the wall-passivating Si_3N_4 layer

Very long etching times due to the length of the pores are expected, because the etching solution has to reach the pore bottom by diffusion. In addition, using the commonly utilized Si_3N_4 etches, i.e. hot phosphoric acid or HF containing etches [25], respectively, is problematic because the Al mask is simultaneously attacked. However, somewhat unexpectedly, a combination of buffered oxide etch (BOE) and a wetting agent (pH $\sim$4.5) passivates the Al after an induction period of 10 min. During this time strong gas bubble evolution takes place due to a chemical reaction. It is related to the removal of the natural oxide layer (Al_2O_3) and Al dissolution. It is important to note that the etch of the Al mask is not completely stopped but the reaction rate is remarkably slowing down after the induction period. This phenomenon is not understood in detail but may be probably due to the formation of an amphoteric aluminum hydroxide layer [$Al(OH)_3$] which is known to be relatively stable against acids [26]. Although the mask is damaged, it is possible to etch samples for about 90 min (!) in such a solution at room temperature. After that time, the Si_3N_4 in 150 μm deep pores is completely removed. There are no significant differences in etching times between the different pore patterns we used. This can be attributed to lower diffusion rates in the smaller pores of pattern B. However, the etch damage of the mask was found to be acceptable in either case for the order of the microstructures we used.

3.6 Microstructure etching process

The etching of the microstructures is performed chemically with a CF_4/O_2 plasma in a Barrel reactor. By doing this there is sufficient selectivity concerning the etching rates of bulk silicon and Si_3N_4. In addition, the Al mask will not be attacked by this plasma. Although barrel etching, in general, is an isotropic process, the anisotropy of the etching, forced by the pore array, is clearly visible in Fig. 6, where a typical microstructure (pattern A) depth profile is shown. As mentioned above, the pore array together with the Si_3N_4 sidewall passivation is responsible for the high anisotropy of the process. For the 140 μm deep structures visualized, an overall etching time of 60 min is required. With pattern B the etching time reduces to 16 min. Although there is no linear relation between etch depth and etching time, one can conclude that the smaller pattern B has improved the etching conditions.

The mask undercut directly depends on the etching time and therefore on the etch depth. In [16] it is shown that some rows of trenches have broken off the wall, resulting in mask undercut in the range of 20 μm for pattern A. For pattern B, the undercut reduces to 12–15 μm. It is found that the smaller array B shortens the etching time but at the same time loses more rows of trenches; however, if we compare the wall steepness, pattern B again shows better results. This is visualized in the next section. The relatively strong undercut is one of the critical limitations of our process and is discussed subsequently in detail. It is also worthwhile to consider other processes for the microstructure etching like RIE or other anisotropic dry-etch methods to optimize the process.

3.7 Pore filling

To get complete, compact microstructures, the pores must be filled. We use a polysilicon deposition process. It is performed with low deposition rate to ensure uniform

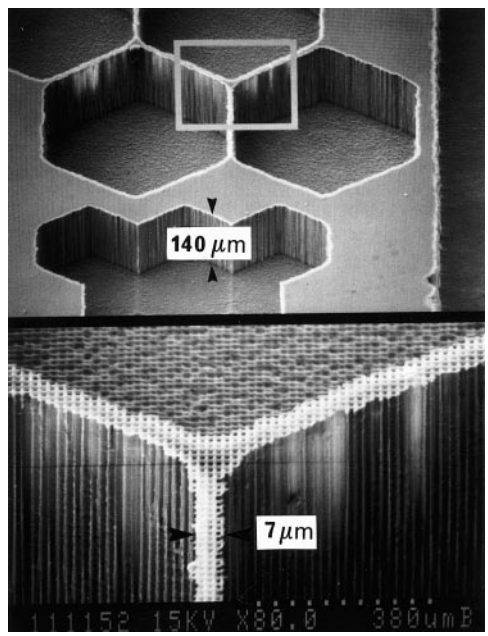

Fig. 6. Microstructure depth profile (pattern A) obtained after 60 min of plasma etch performed in several steps of 5 and 10 min, respectively, and removal of the Al mask.

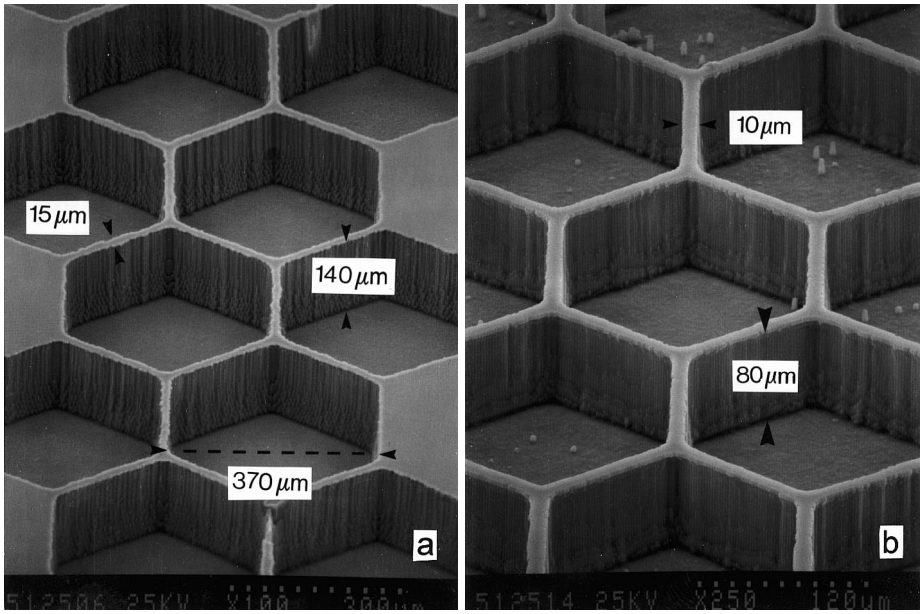

Fig. 7a, b. Microstructures obtained after pore filling with polysilicon: (**a**) 140 μm deep structures on pattern A, (**b**) 80 μm deep structures on pattern B. It is clearly visible that pattern B resolves the microstructures better (see scaling!)

polysilicon deposition over the whole pore depth. Figure 7a and b shows some results for samples produced on patterns A and B, respectively. The resolution of the structures is much better with the smaller array B. Figure 8 shows an example for the excellent steepness of the pore walls of pattern B. Although the surface is completely covered with polysilicon, it can be seen from Figs. 8 and 9, where a 45° bevel was cut on the sample, that the pores are not completely filled over the whole depth. Figure 7a and b also shows that the polysilicon deposition process results in a relatively rough surface. It is so far very difficult to use these structures for molding or electroplating, respectively, because much more smoother surfaces are required for that. Further work is needed to optimize this process or develop other pore-filling techniques.

4 Limitations of the process and future work

As mentioned above, the process is limited to low-doped *n*-type silicon with (100) orientation, due to the generation of the pore array. It is the basis of the process and could not be created on selected places on a sample. Always the whole sample exposed to the electrolyte is etched with a constant porosity. The pore array causes another problem: Since *n*-type silicon with particular orientation is required for pore etching, it is, for instance, not possible to work with sacrificial layers to remove the microstructures from the bulk material or to create movable tools. However, this could probably be circumvented by developing suitable molding techniques, although at the moment the sidewall roughness is too high.

Work is in progress to reduce costs by trying to extend the accuracy of the etching process with "wild pores", i.e. pores that are randomly grown without any pore pattern. It is possible to produce pores of equal length without using photolithography. The problem so far is the reproducible adjustment of pore geometry, i.e. the number of pores, their diameter and their spacing.

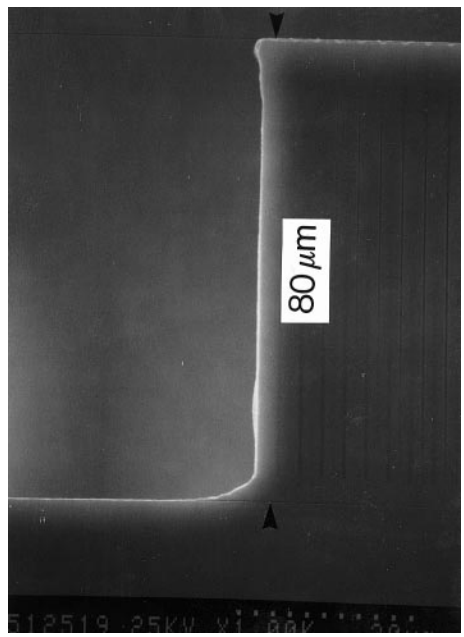

Fig. 8. Example for the excellent wall steepness obtained by using pattern B

The mask undercut has to be taken into account in designing the microstructures. For a sample with pattern A, i.e. with a structure height of 150 μm, the mask undercut is nearly 20 μm. This means that mask structures smaller than 40 μm are critical for depth profile etching of roughly 150 μm in this technology. The use of pattern B only apparently reduces the undercut. The structure height is 80 μm, whereas the mask undercut is nearly 12–15 μm. A real improvement is reached in microstructure resolution and the entire etching time by using the smaller pore pattern. It can be seen that irregularities at the side-walls are directly connected to the dimensions of

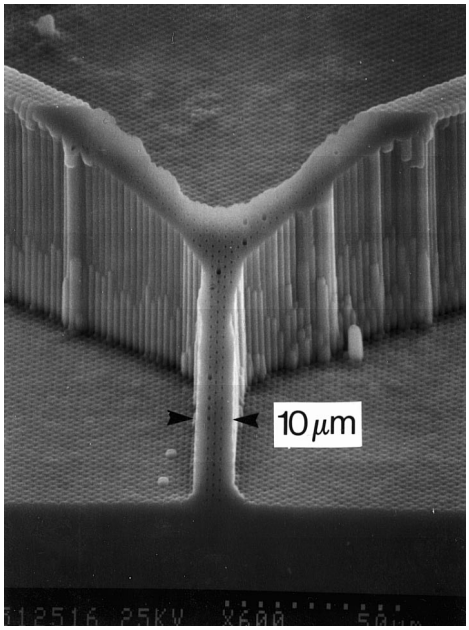

Fig. 9. Beveling (45°) of the sample shown in Fig. 7b visualizes that the pores are not completely filled

the pore pattern. Using pore arrays in the submicrometer range is a promising attempt for resolution improvement of the microstructures.

5 Conclusion

A micromachining process for silicon with steep sidewalls and high aspect ratios of 10–15 has been developed. The process is fully compatible with standard microelectronic processes. It is based on well-oriented macropore arrays in *n*-type silicon substrates, which are obtained by electrochemical etching in HF electrolyte. The pores facilitate the anisotropy of the microstructure etching process; therefore, an isotropic etch process is sufficient. Different pore patterns concerning pore spacing, pore diameter and geometry were used. It is demonstrated that smaller arrays improve the microstructure resolution; however, the sidewall roughness is so far too high for electroplating and molding. By further reducing the pore array parameters and by improvement of the pore-filling technique, it should be possible to produce smoother surfaces to facilitate molding of the structures.

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