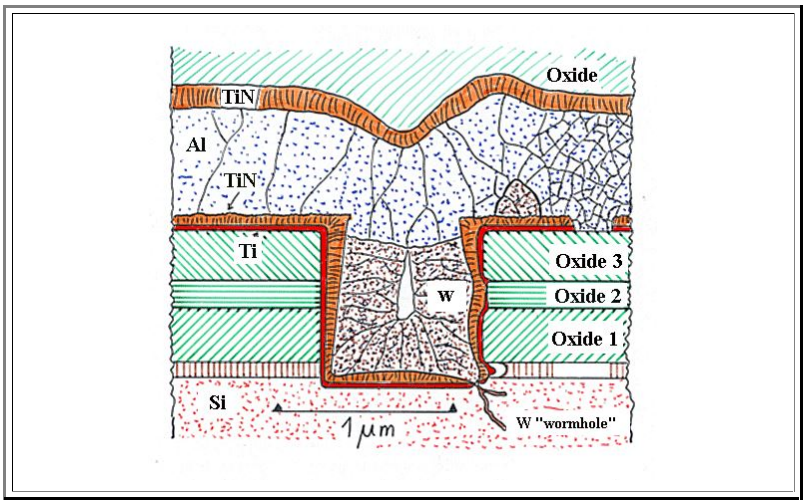
6.5 Etching Techniques

6.5.1 General Remarks

- After we have produced all kinds of layer, we must now proceed to the structure module of our basic process cycle. First we discuss **etching techniques**.
  - Lets see what it means to produce a structure by etching. Lets make, e.g., a contact hole in a somewhat advanced process (and do some of the follow-up processes for clarity).
  - What the stucture contains may look like this:

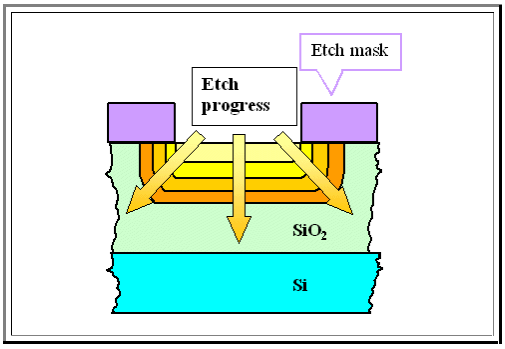


- Obviously, before you deposit the **Ti/TiN** diffusion barrier layer (and then the **W**, and so on), you must etch a hole through **3** oxide layers and an **Si_3N_4** - and here we don't care why we have all those layers. (The right hand side of the picture shows a few things that can go wrong in the contact making process, but that shall not concern us at present).
- There are some obvious requirements for the etching of this contact hole that also come up for most other etching processes.
  - **1.** You only want to etch *straight down* - not in the lateral direction. In other words, you want strongly **anisotropic etching** that only affects the bottom of the contact hole to be formed, but not the sidewalls (which are, after all, of the same material).
  - **2.** You want to *stop* as soon as you reach the **Si** substrate. Ideally, whatever you do for etching will not affect **Si** (or whatever material you want not to be affected). In other words, you want a large **selectivity** (**=** ratio of etch rates).
  - **3.** You also want reasonable *etching rates* (time is money), the ability to etch through several *different* layers in *one* process (as above), no *damage* of any kind (including rough surfaces) to the layer where you stop, and sometimes *extreme* geometries (e.g. when you etch a trench for a capacitor: **0,8 µm** in diameter and **8 µm** deep) - and you want perfect *homogeneity and reproducibility* all the time (e.g. all the about **200.000.000.000** trenches on *one* **300 mm** wafer containg **256 Mbit DRAMs** must be identical to the ones on the other ***500 - 1000*** wafers you etch today, *and* to the *thousands* you etched before, or are going to etch in the future).
- Lets face it: *This is tough*! There is no single technique that meets all the requirements for all situations.
  - Structure etching thus is almost always a search for the best compromise, and new etching techniques are introduced all the time.
  - Here we can only scratch at the surface and look at the two basic technologies in use: *Chemical or wet etching* and *plasma or dry etching*.

6.5.2 Chemical Etching

- Chemical etching is simple: Find some (liquid) chemical that dissolves the layer to be etched, but that does not react with everything else.
  - Sometimes this works, sometimes it doesn`t. Hydrofluoric acid (**HF**), for example will dissolve **SiO_2**, but not **Si** - so there is an etching solution for etching **SiO_2** with extreme selectivity to **Si**.
  - The other way around does not work: Whatever dissolves **Si**, will always dissolve **SiO_2**, too. At best you may come up with an etchant that shows somewhat different etching rates, i.e. some (poor) selectivity.

- Anyway, the thing to remember is: Chemical etchants, if existing, can provide extremely good selectivity and thus meet our *second* request from above.
  - How about the *first* request, anisotropy? Well, as you guessed: It is rotten, practically non-existent. A chemical etchant always dissolves the material it is in contact with, the forming of a contact hole would look like this:



- There is a simple and painful consequence: As soon as your feature size is about **2 µm** or smaller, *forget chemical structure etching*.
  - Really? How about making the opening in the mask smaller, accounting for the increase in lateral dimensions?
  - You could do that - it would work. But it would be foolish: If you *can* make the opening smaller, you also want your features smaller. In real life, you put up a tremendous effort to make the contact hole opening as small as you can, and you sure like hell don't want to increase it by the structure etching!
- Does that mean that there is no chemical etching in **Si** microelectronics? Far from it. There just is no chemical *structure* etching any more. But there are plenty of opportunities to use chemical etches (cf. the statistics to the **16 Mbit DRAM** process). Lets list a few:
  - *Etching off whole layers*. Be it some sacrificial layer after it fulfilled its purpose, the photo resist, or simply all the **CVD** layers or thermal oxides which are automatically deposited on the wafer backside, too - they all must come off eventually and this is best done by wet chemistry.
  - Etching *coarse structures*, e.g. the opening in some protective layers to the large **Al** pads which are necessary for attaching a wire to the outside world.
  - Etching off unwanted *native oxide* on all **Si** or poly-**Si** layers that were exposed to air for more than about **10 min**.
  - All *cleaning steps* may be considered to be an extreme form of chemical etching. Etching off about **1,8 nm** of native oxide might be considered cleaning, and a cleaning step where nothing is changed at the surface, simply has no effect.
- While these are not the exciting process modules, experienced process engineers know that this is where trouble lurks. Many factories have suffered large losses because the yield was down - due to some problem with wet chemistry.
- A totally new field, just making it into production for some special applications, is **electrochemical etching**. A few amazing (and not yet well understood) things can be done that way; the link provides some samples.