6.4. Physical Processes for Layer Deposition

- The technologies discussed in this subchapter essentially cover *physical processes* for layer deposition as opposed to the more *chemical* methods introduced in the preceding subchapters. In other words, we deal with some more techniques for the material module in the process cycle for **ICs**.
  - While still intimately tied to the electronic materials to be processed, these technologies are a bit more of a side issue in the context of electronic materials, and will therefore be covered in *far less detail* then the preceding, more material oriented deposition techniques.
  - On occasion, however, a particular tough problem in **IC** processing is elucidated in the context of the particular deposition method associated with it. *So don't skip these modules completely!*
- Essentially, what you should know are the basic technologies employed for layer deposition, and some of the major problems, advantages and disadvantages encountered with these techniques in the context of chip manufacture.

6.4.1 Sputter Deposition and Contact Hole Filling

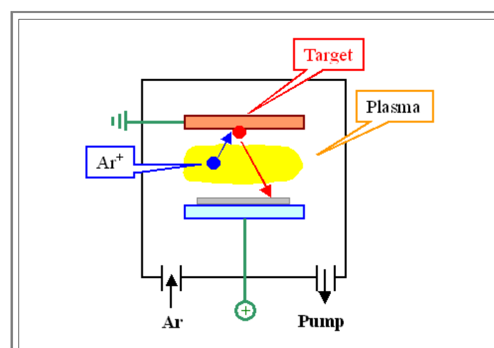
General Remarks

- It should be clear by now that the *deposition of thin layers* is the key to all microelectronic structures (not to mention the emerging micro electronic and mechanical systems (**MEMS**), or **nano technology**).
  - *Chemical* vapor deposition, while very prominent and useful, has severe limitations and the more alternative methods exist, the better.
  - *Physical* methods for controlled deposition of thin layers do exist too; and in the remainder of his subchapter we will discuss the major ones.
- What are *physical* methods as opposed to *chemical* methods? While there is no ironclad distinction, we may simply use the following rules
  - If the material of the layer is produced by a *chemical reaction* between some primary substances in-situ, we have a chemical deposition process. This does not just include the **CVD** processes covered before, but also e.g. galvanic layer deposition.
  - If the material forming the layer is sort of transferred from some substrate or source to the material to be coated, we have a *physical process*. The most important physical processes for layer deposition which shall be treated here are

    - **Sputtering techniques**
    - **Ion implantation**
    - **Spin on coating**

Basic Sputter Process

- "**Sputtering**" or "**sputter deposition**" is a conceptually simple technique:
  - A "**target**" made of the material to be deposited is bombarded by energetic ions which will dislodge atomes of the target, i.e., "***sputter*** them off".
  - The dislodged atoms will have substantial kinetic energies, and some will fly to the substrate to be coated and stick there.
- In practice, this is a lot easier than it appears. The basic set-up is shown below:



- The ions necessary for the bombardment of the target are simply extracted from an **Ar plasma** burning between the target and the substrate.

- Both target and substrate are planar plates arranged as shown above. They also serve as the cathode and anode for the gas discharge that produces an **Ar** plasma, i.e. ionized **Ar** and free electrons, quite similar to what is going on in a fluorescent light tube.
- Since the target electrode is always the cathode, i.e. negatively charged, it will attract the Ar^+ ions and thus is bombarded by a (hopefully) constant flux of relatively energetic **Ar** ions.
- This ion bombardment will liberate atoms from the target which issue forth from it in all directions.

Reality is much more complex, of course. There are many ways of generating the plasma and tricks to increase the deposition rate. Time is money, after all, in semiconductor processing.
Some target atoms will make it to the substrate to be coated, others will miss it, and some will become ionized and return to the target. The important points for the atoms that make it to the substrate (if everything is working right) are:

- **1.** The target atoms hit the substrate with an energy large enough so they "*get stuck*", but not so large as to liberate substrate atoms. Sputtered layers therefore usually stick well to the substrate (in contrast to other techniques, most notably evaporation).
- **2.** *All* atoms of the target will become deposited, in pretty much the same composition as in the target. It is thus possible, e.g., to deposit a silicide slightly off the stoichiometric composition (advantageous for all kinds of reason). In other words, if you need to deposit e.g. $TaSi_{2-x}$ with $x \approx 0.01 - 0.1$, sputtering is the way to do it because it is comparatively easy to change the target composition.
- **3.** The target atoms hit the substrate coming from *all directions*. In a good approximation, the flux of atoms leaving the target at an angle Φ relative to the normal on the target is proportional to $\cos\Phi$. This has profound implications for the coverage of topographic structures.
- **4.** Homogeneous coverage of the substrate is relatively easy to achieve- just make the substrate holder and the target big enough. The process is also relatively easily scaled to larger size substrates - simply make everything bigger.

Of course, there are problems, too.

- Sputtered layers usually have a very bad crystallinity - very small grains full of defects or even amorphous layers result. Usually some kind of annealing of the layers is necessary to restore acceptable crystal quality.
- Sputtering works well for metals or other somewhat conducting materials. It is not easy or simply impossible for insulators. Sputtering SiO_2 layers, e.g., has been tried often, but never made it to production.
- While the $\cos\Phi$ relation for the directions of the sputtered atoms is great for over-all homogeneity of the layers, it will prevent the filling of holes with large **aspect ratios** (aspect ratio **=** depth/width of a hole). Since contact holes and vias in modern **ICs** always have large aspect ratios, a serious problem with sputtering A**l(Si Cu)** for contacts came up in the nineties of the last century. This is elaborated in more detail below.

More or less by default, sputtering is the layer deposition process of choice for **Al**, the prime material for metallization.

- How else would you do it? Think about it. We already ruled out **CVD** methods. What is left?
- The deposition of a metallization layer on a substrate with "heavy" topography - look at some of the drawings and pictures to understand this problem - is one of the big challenges **IC** technology and a particularly useful topic to illustrate the differences between the various deposition technologies; it will be given some special attention below.

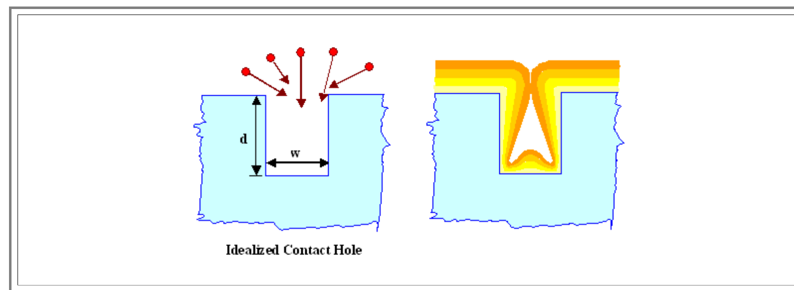
The Contact Hole Problem

The metallization of chips for some **30** years was done with Aluminum as we know by now - cf. all the drawings in chapter 5 and the link.

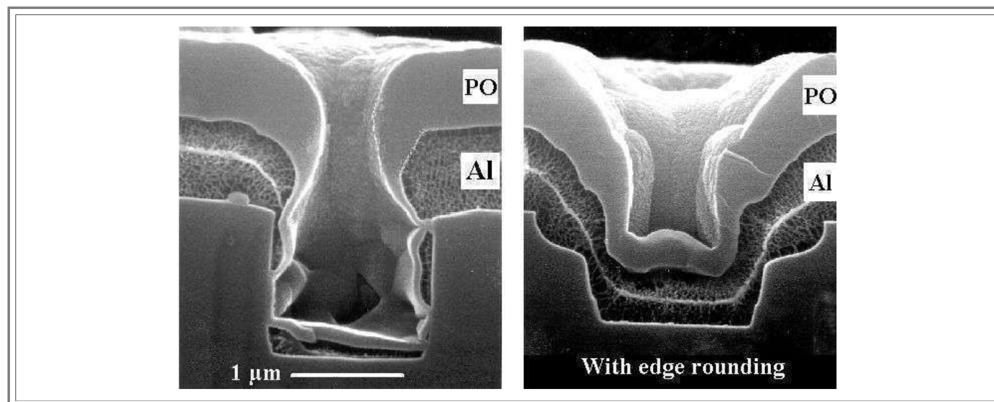
- **Al**, while far from being optimal, had the best over-all properties (or the best "figure of merit") including less than about **0,5 % Si** and often a little bit (roughly **1 %**) of **Cu**, **V** or **Ti**. These elements are added in order to avoid deadly "spikes", to decrease the contact resistance by avoiding epitaxial Si precipitates and to make the metallization more resistant to electromigration.
- While you do not have to know what that means (you might, however, look it up via the links), you should be aware that there are even more requirements for a metallization material than listed before.

Sputtering is the only process that can deposit an **Al** layer with a precisely determined addition of some other elements on a large **Si** substrate. There is an unavoidable problem however, that becomes more severe as features get smaller, related to the so-called "edge coverage" of deposition processes.

- Many **Al** atoms hitting the substrate under an oblique angle, will not be able to reach the bottom of a contact hole which thus will have less Al deposited as the substrate surface.
- To make it even worse, the layer at the edge of the contact hole tends to be especially thick, reducing the opening of the hole disproportionately and thus allowing even less **Al** atoms to bottom of the hole. What happens is illustrated below.



- Fort aspect ratios ***A* = *w/d*** smaller than approximately **1**, the layer at the edge of the contact hole will become unacceptably thin or will even be non-existing - the contact to the underlying structure is not established.
  - The real thing together with one way to overcome the problem is shown below (the example is from the **4Mbit DRAM** generation, around **1988**).



  - ***PO*** denotes "**Plasma oxide**", referring to a PECVD deposition technique for an oxide. This layer is needed for preparation purposes (the upper **Al** edge would otherwise not be clearly visible)
- Clearly, the **Al** layer is interrupted in the contact hole on the left. **Al** sputter deposition cannot be used anymore without "tricks".
  - One possible trick is shown on the right: The edges of the contact hole were "rounded". "**Edge rounding**", while not easy to do and consuming some valuable "real estate" on the chip, saved the day for the at or just below the **1µm** design rules.
  - But eventually, the end of sputtering for the **1st** metallization layer was unavoidable - despite valiant efforts of sputter equipment companies and **IC** manufacturers to come up with some modified and better processes - and a totally new technology was necessary
- This was **Tungsten CVD** just for filling the contact hole with a metal.
  - In some added process modules, the wafer was first covered with tungsten until the contact holes were filled (cf. the drawing in the **CVD** module). After that, the tungsten on the substrate was polished off so that only filled contact holes remained.
  - After that, **Al** could be deposited as before.
- However, depositing **W** directly on **Si** produced some new problems; related to interdiffusion of **Si** and **W**.
  - The solution was to have an intermediary **diffusion barrier** layer (which was, for different reasons, already employed in some cases with a traditional **Al** metallization).
  - Often, this diffusion barrier layer consisted of a thin **$TiSi_2$/Ti /TiN** layer sequence. The **$TiSi_2$** formed directly as soon as **Ti** was deposited (by sputtering, which was still good enough for a very thin coating), the **Titanium Nitride** was formed by a **reactive sputtering process**.
  - Reactive sputtering in this case simply means that some **N_2** was admitted into the sputter chamber which reacts immediately with freshly formed (and extremely reactive) **Ti** to **TiN**.
- A typical contact to lets say **p**-type **Si** now consisted of a **p-Si/p^+-Si/$TiSi_2$/Ti/TiN/W/Al** stack, which opened a new can of worms with regard to contact reliability. Just imagine the many possibilities of forming all kinds of compounds by interdiffusion of whatever over the years.
  - But here we stop. Simply because meanwhile (i.e. **2001**), contacts are even more complicated, employing **Cu** (deposited galvanically after a thin **Cu** layer necessary for electrical contact has been sputter deposited), various barrier layers, possibly still **W**, and whatnot.
  - So: Do look at a modern chip with some awe *and remember*: We are talking electronic materials here!

Questionaire
Multiple Choice questions to 6.4.1