## 5.5.1 Summary: General Aspects of Silicon Technology

Essentials of the bipolar transistor:

- High emitter doping (N_{Don} for **npn** transistor here) in comparison to base doping N_{Ac} for large current amplification factor $\gamma = I_C/I_B$.

- $N_{Don}/N_{Ac} \approx \kappa =$ injection ratio.

$$\gamma \approx \frac{N_{Don}}{N_{Ac}} \cdot \left(1 - \frac{d_{base}}{L} \right)$$

- Small base width d_{base} (relative to diffusion length L) for large current amplification.
- Not as easy to make as the band-diagram suggests!
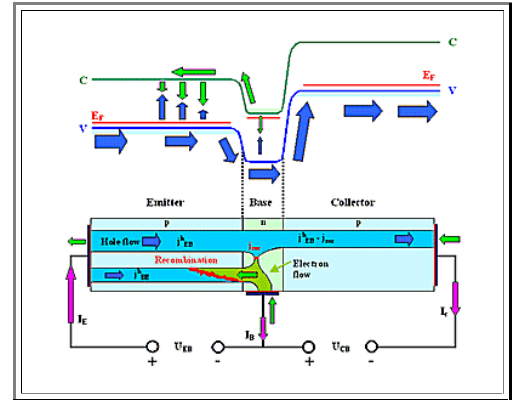
Essentials of the MOS transistor:

- Gate voltage enables Source-Drain current

- Essential process. Inversion of majority carrier type in channel below gate by:

  - Drive intrinsic majority carriers into bulk by gate voltage with same sign as majority carriers.
  - Reduced majority concentration n_{maj} below gate increases minority carrier concentration n_{min} via mass action law

$$n_{maj} \cdot n_{min} = n_i^2$$

Band diagram for inversion

  - An inversion channel with $n_{min} > n_{maj}$ develops below the gate as soon as threshold voltage U_{Th} is reached.
  - Current now can flow because the reversely biased **pn**-junction between either source or drain and the region below the gate has disappeared.
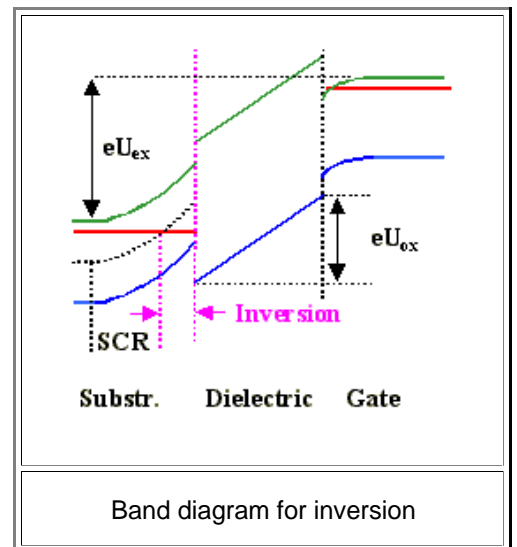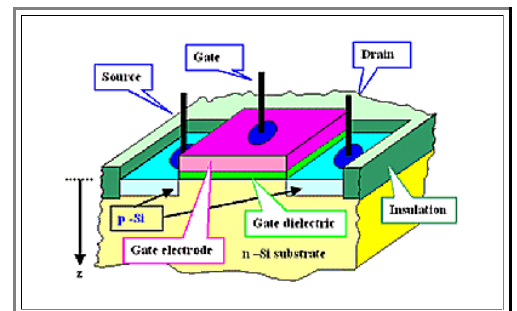
The decisive material is the gate dielectric (usually SiO$_2$). Basic requirement is:

- High capacity C_G of the gate electrode - gate dielectric - **Si** capacitor = high charge Q_G on electrodes = strong band bending = low threshold voltages U_G

$$Q_G = C_G \cdot U_G$$

- It follows:

Example:
$U = 5$ V, $d_{Di} = 5$ nm $\Rightarrow E = U/d_{Di} = 10^7$ V/cm **!!**

$\epsilon_r(SiO_2) = 3.9$

  - Gate dielectric thickness $d_{Di} \Rightarrow$ High breakdown field strength U_{Bd}
  - Large dielectric constant ϵ_r
  - No interface states.
  - Good adhesion, easy to make / deposit, easy to structure, small leakage currents, ...

Integration means:

- **1.** Produce a large number (up to **1.000.000.000**) of transistors (bipolar or **MOS**) and other electronic elements on a **cm^2** of **Si**
- **2.** Keep thoses elements electrically insulated from each other.
- **3.** Connect those elements in a meaningful way to produce a system / product.

It ain't easy!

An integrated bipolar transistor does not resemble the textbook picture at all, but looks far more complicated ⇒.

- This is due to the insulation requirements, the process requirements, and the need to interconnect as efficiently as possible.

- The epitaxial layer cuts down on the number of critical diffusions, makes insulation easier, and allows a "buried contact" structure.
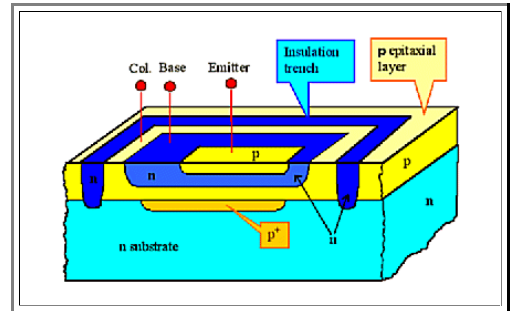

Connecting transistor / elements is complicated; it has to be done on several levels

- Materials used are **Al** ("old"), **Cu** ("new"), **W**, (highly doped) poly-**Si** as well as various silicides.

- Essential properties are the conductivity σ of the conductor, the dielectric constant ϵ_r of the intermetal dielectric, and the resulting time constant $\tau = \sigma \cdot \epsilon_r$ that defines the maximum signal transmision frequency through the conducting line.
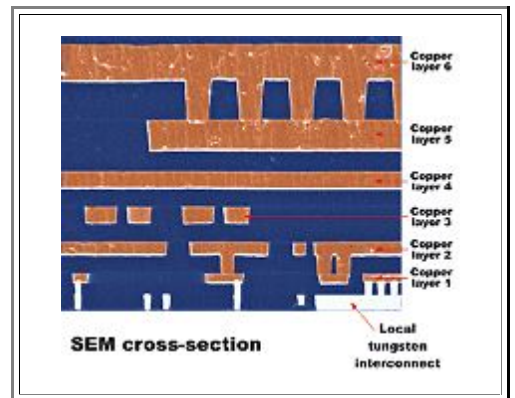

Integrating **MOS** transistors requires special measures for insulation (e.g. a field oxide) and for gate oxide production

- Since a **MOS** transistor contains intrinsically a capacitor (the gate "stack"), the technology can be used to produce capacitors, too.
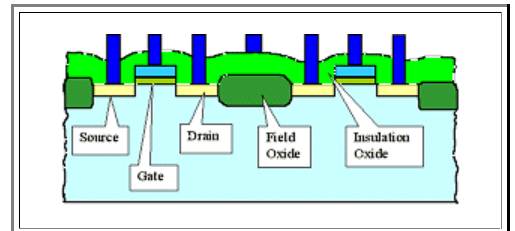

CMOS allows to reduce power consumption dramatically.

- The process, however, is more complex: Wells with different doping type need to be made.
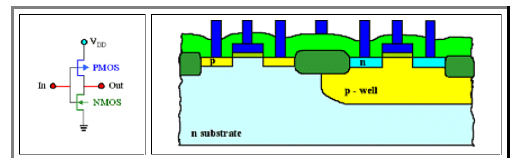
Using the third dimension (depth / height) might become necessary for integrating "large" structures into a small projected are (example: trench capacitor in **DRAMs** ⇒).

- Unwanted "topology", however, makes integration more difficult.

- Planarized technologies are a must since about 1995! ⇒

Non-planarized 16M DRAM   **Planarized 64M DRAM**
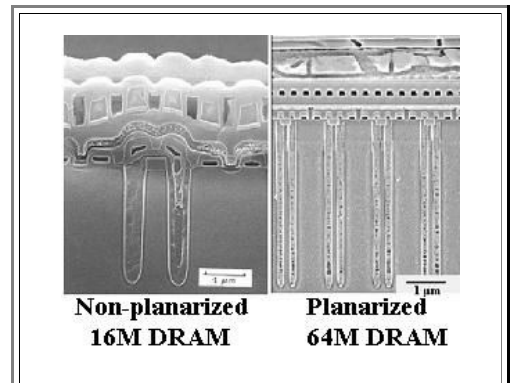
It ain't neither easy nor cheap!

Property	Number
Feature size	**0,2 µm**
No. metallization levels	**4 - 7**
No. components	**> 6 · 10^8 (Memory)**
Complexity	**> 500 Process steps**
Cost (development and **1** factory)	**ca. $ 6 · 10^9**

Typical wafer size for new factories (**2007**) : **300 mm** diameter, **775 µm** thickness, flatness in lower **µm** region

- Chip size a few **cm^2**, much smaller if possible
- Yield **Y** = most important parameter in chip production = % of chips on a wafer that function (= can be sold).
- **Y = 29 %** is a good value for starting production

Chip making = running about **20** times (roughly!!) through "materials" - "structuring" loop.

- About **400 - 600** individual processing steps (= in / out of special "machine") before chip is finished on wafer
- More than **30** processing steps for packaging (after separation of chips by cutting)
- Simple estimate: **99.9%** perfection for each processing step means **Y < 70 %.**

Dirt in any form - as "particles" on the surface of wafer, or as "contamination" inside the wafer is almost always deadly

- Particles with sized not much smaller than minimum feature sizes (i.e. < **10 nm** in **2007**) will invariably cover structures and lead to local dysfunction of a transistor or whatever.
- Point defects like metal atoms in the **Si** lattice may precipitate and cause local short circuits etc. from the "inside", killing transistors
- One dysfunctional transistor out of **1.000.000.000** or so is enough to kill a chip!

Being extremely clean is absolutely mandatory for high Yields **Y**!

- Use cleanrooms and hyper-clean materials!
- It won't be cheap!
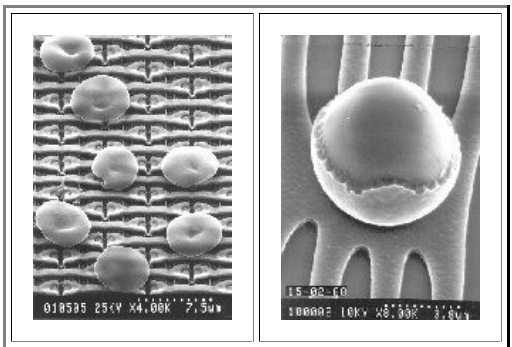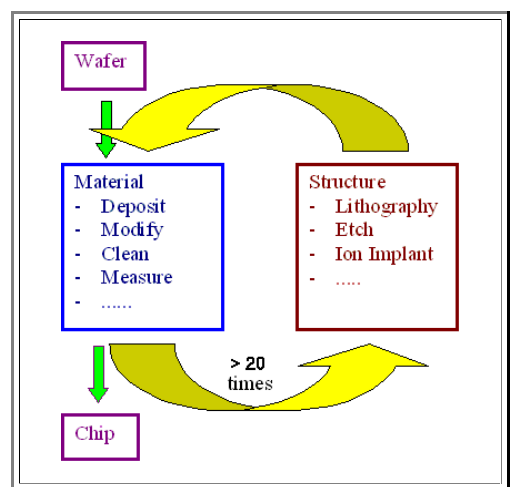
- Moore's law predicts exponentially growth of "chip complexity" with a high growth rate - how far will it reach?
  - Problems and costs are growing exponentially with every new generation.
  - It follows: The market must grow exponentially too, if you want to make a profit.
  - It follows: Large amounts of money can be easily made - or lost.
- Falling behind thecompetition in your technology and yields means certain death for companies without a monopoly in some product.
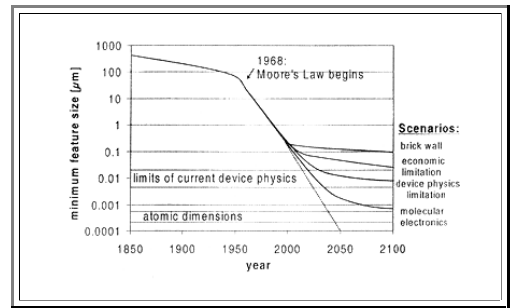
| **Questionaire** |
| **Multiple Choice questions to all of 5** |