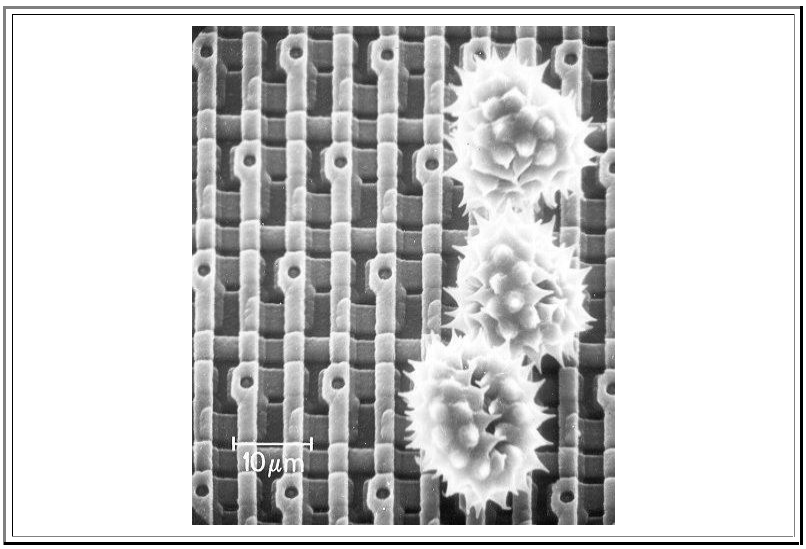
5.3 Cleanrooms, Particles and Contamination

5.3.1 Cleanrooms and Defects

Particles

- Normal air is full of "dirt" usually called **particles**. The fact that *we* cannot see them (except the bigger ones in a bright beam of light) does not mean that the air is clean. What happens when a particle (e.g. pollen, scrapings from whatever, unknown things) falls on a chip is shown in the picture below.
  - Anything that can "fall" on a chip is called a *particle*; independent of its size and of what it is. Particles smaller than some **10 µm** usually do not "feel" gravity anymore (other forces dominate); so they do not "fall" on a chip. However, they may be attracted electrostatically and that makes it quite difficult to remove them.
  - Often anything that disturbs the structure of a chip by lying *on* the layers of the integrated circuit is called a **"defect"**. Defects may not only be particles, but all kinds of other mishaps too, e.g. small holes in some coating.
  - However, we will *not* use that terminology here, but restrict the name "*defect*" to **crystal lattice defects** *in* the **Si**, i.e. *in*, not *on*, the integrated circuit.
  - A pretty old chip (a **256k** memory as sold around **1985**) was chosen for the following illustration because its structures are clearly visible. It has a few pollen grains (from "Gänseblümchen") on its surface (which essentially shows the wiring matrix of a memory array). What would have happened if a pollen grain would have fallen on the chip while it was made needs no long discussion: The chip would be dead!

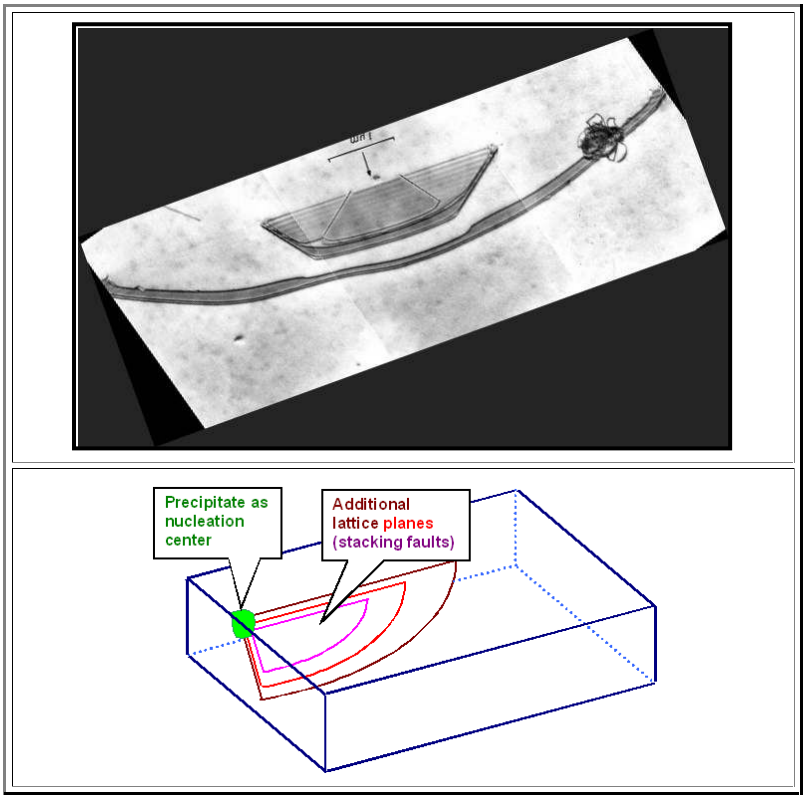


- At feature sizes **< 0,2 µm**, everything that falls on a chip with sizes **> 0,1 µm** or so will be deadly. All those defects- the **particles** - must be avoided at all costs. There are three major sources of particles:
- **1.** The *air* in general. Even "clean" mountain air contains very roughly 10^6 particles **> 1 µm** per *cubic foot* (approximately **30** liters). We need a "**cleanroom**" serving two functions:
  - It provides absolutely clean air (usually through filters in the ceiling), and
  - It immediately removes particles generated somewhere in the cleanroom by pumping large amounts of clean air from the ceiling through the (perforated) floor.
  - Avoiding and removing particles while processing **Si** wafers has grown into a science and industry of its own. The link provides some information about cleanrooms and cleanroom technology.
- **2.**The *humans* working in the cleanroom.
  - Wiping your (freshly washed) hair just once, will produce some **10 000** particles. If you smoke, you will exhale thousands of particles (size about **0,2 µm**) with every breath you take. A ***TI*** add once said: Work for us and we will turn you into a non-smoker.
  - The solution is to pack you into **cleanroom garments**; what this looks like can be seen in the link. It is not as uncomfortable as it looks; but it is not pure fun either. Graphic examples of humans as a source of particles can be found in the link.
- **3.** The *machines* (called "**equipment**") that do something to the chip, may also produce particles.
  - As a rule, *whenever something slides on something else* (and this covers most mechanical movements), particles are produced. Layers deposited on chips are also deposited on the inside of the equipment; they might flake off. There is no easy fix, but two rules:
  - - Use special engineering and construction to avoid or at least minimize all possible particle sources, and
    - Keep your equipment clean - frequent "special" cleaning is required!

- But even with state-of-the art cleanrooms, completely covered humans, and optimized equipment, particles can not be avoided - look at the picture gallery to get an idea of what we are up to. The most frequent process in chip manufacture therefore is "cleaning" the wafers.
  - Essentially, the wafers are immersed in special chemicals (usually acids or caustics or in combination with various special agents), agitated, heated, rinsed, spin-dried, ... , its not unlike a washing machine cycle.
  - This cleaning process in all kinds of modifications is used not only for removing particles, but also for removing unwanted atoms or layers of atoms which may be on the surface of the wafers. This brings us to the next point:

Contamination and Crystal Lattice Defects

- The **Si** single crystals used for making integrated circuits are the (thermodynamically) most perfect objects in existence - at least on this side of Pluto. They are in particular completely free of dislocations and coarser defects as, e.g., grain boundaries or precipitates of impurities, and have impurity concentrations typically in the **ppt** (parts per trillion) or **ppqt** (parts per quadrillion) range - many orders of magnitude below of what is normally considered "high-purity".
- *Defects* (always now in the meaning of "*crystal lattice defects*") will without fail kill the device or change properties!
  - *Dislocations* or *precipitates* in the electronically active region of the device; e.g. in or across **pn**-junctions, simply "kill" it - the junction will be more or less short-circuited.
  - *Point defects* in solid solution (e.g. **Cu**, **Au**, **Fe**, **Cr**, ...most metals) in the **Si** crystal reduce the *minority carrier lifetime* and thus influence device characteristics directly - usually it will be degraded. Alkali atoms like **Na** and **K** in the gate oxides kill **MOS** transistors, because they move under the applied electrical field and thus change the charge distribution and therefore the transistor characteristics.
  - But point defects do more: If they precipitate (and they all have a tendency to do this because their solubility at low temperatures is low) close to a critical device part (e.g. the interface of **Si** and SiO_2 in the **MOS** transistor channel), they simply kill that transistor. Possibly worse: Even very small precipitates of impurities may act as the nuclei for large defects, e.g. dislocations or stacking faults, that without help at the nucleation stage would not have formed.
- This simply means that we have to keep the **Si**-crystal free of so-called **process-induced defects** during processing, something not easily achieved. Cleaning helps in this case, too.
  - Below a picture of what a process-induced defect may look like. It was taken by a *transmission electron microscope* (***TEM***) and shows the projection of a systems of stacking faults (i.e. additional lattice planes bounded by dislocations) extending from the surface of the wafer into the interior. The schematic picture outlines the three-dimensional geometry



- The central ***precipitate*** that nucleated the stacking fault system is visible as a black dot. The many surplus **Si** atoms needed to form the excessive lattice planes were generated during an oxidation process.
  - Oxidation liberates **Si** interstitials which, since in supersaturation, tend to agglomerate as stacking faults.
  - However, without "help", the nucleation barrier for forming an extended defects can not be overcome, the interstitials then diffuse into the bulk of the crystal were they eventually become immobile and are harmless.
- Defects like the one above are known as "**oxidation induced stacking faults**" or ***OSF***. They form in large densities if even trace amounts of several metals are present which may form precipitates. In order to provide enough metal atoms, it is sufficient to hold the wafer just once with a metal tweezer and subject it to a high temperature process afterwards.
- There are many more ways to generate lattice defects, but there are two golden rules to avoid them:
  - *1. Keep the crystal clean!*
    Even **ppt** of **Fe**, **Ni**, **Cr** (i.e. stainless steel) **Cu**, **Au**, **Pt** or other notorious metals will, via a process that may develop through many heat cycles, eventually produce large defects and kill the device.
  - *2. Keep temperature gradients low!*
    Otherwise mechanical stress is introduced which, if exceeding the yield strength of **Si** (which decreases considerably if impurity precipitates are present), will cause plastic deformation and thus the introduction of large amounts of **dislocations**, which kill your device.
- Via the link a gallery of **process-induced defects** can be accessed together with short comments to their nature and how they were generated.

- There is a simple lecture that can be learned from this: *Electronic Materials* in the context of microelectronics comprise not only the semiconductors, but
  - Anything that can be found in the finished product - the casing (plastics, polymers. metal leads, ..), the materials on and in the **Si**, the **Si** or **GaAs** or... .
  - Anything directly used in making the chip - materials that are "sacrificial", e.g. layers deposited for a particular purpose after which they are removed again, the wet chemicals used for cleaning and etching, the gases, etc.
  - Anything used for handling the chip - the mechanisms that hold the **Si** in the apparatus or transport it, tweezers, etc.
  - Anything in contact with these media - tubing for getting gases and liquids moved, the insides of the processing equipment in contact with the liquid or gaseous media, e.g. furnace tubes.
  - Anything in possible contact with these parts - and so on! It never seems to end - make one mistake (the wrong kind of writing implement that people use in the cleanroom to make notes (not on (dusty) paper, of course, but on clean plastic sheets) - and you may end up with non-functioning chips.
- The link provides a particularly graphic example of how far this has to go!