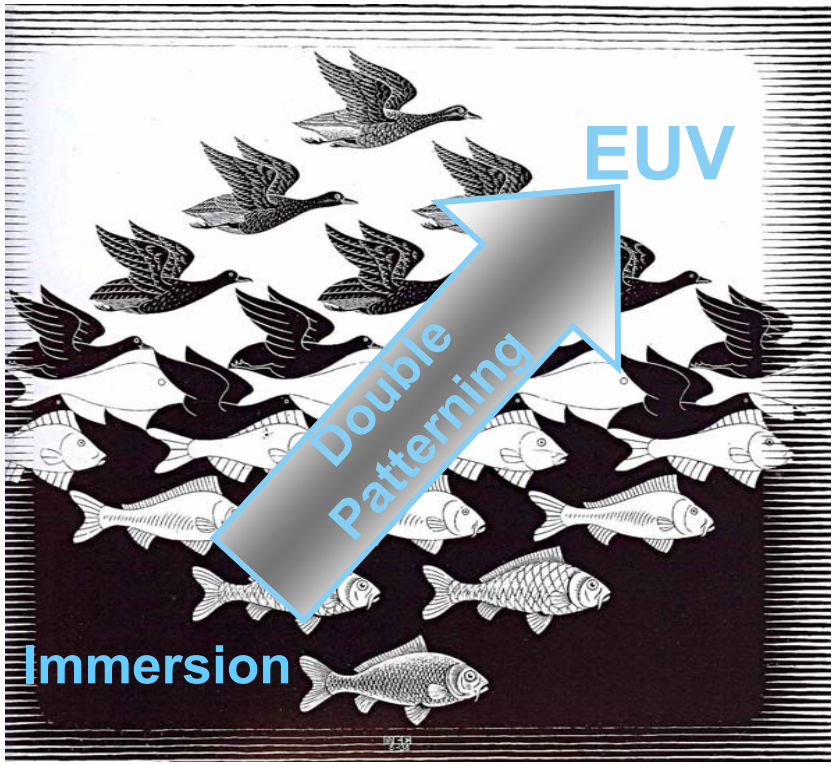
Shrink, an expanding (litho) market

Martin van den Brink

Executive Vice President Marketing and Technology

ISS, Half Moon Bay, Jan 9, 2007

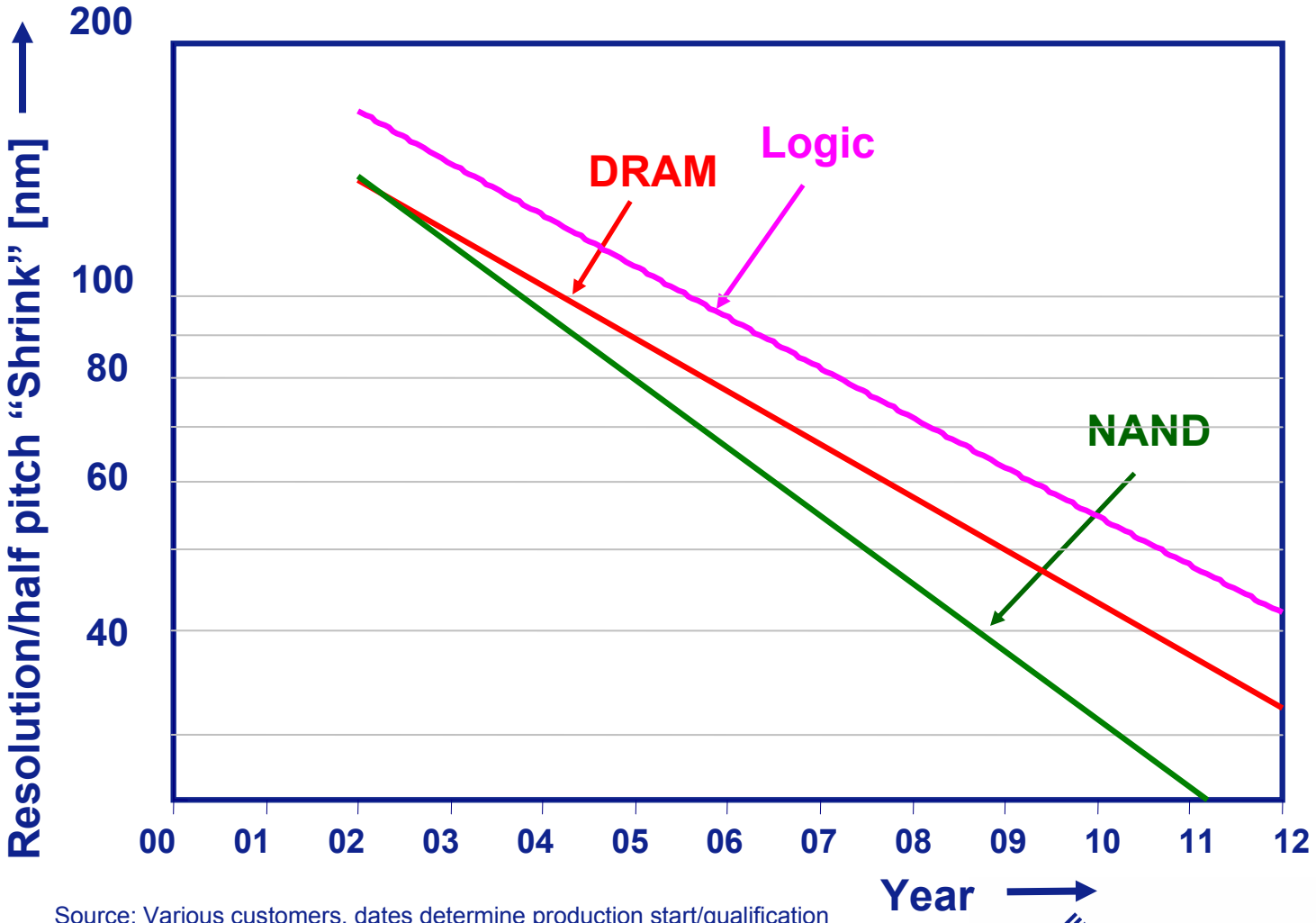


MC Escher

Content

- The demand for shrink continues
- Litho roadmap
- Litho integration
- Litho cost
- Summary

Shrink rates for Logic, DRAM, and NAND flash



Source: Various customers, dates determine production start/qualification

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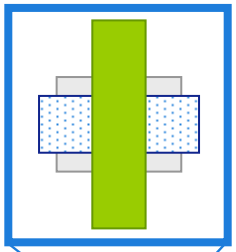
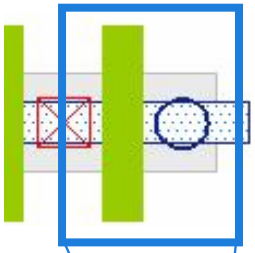
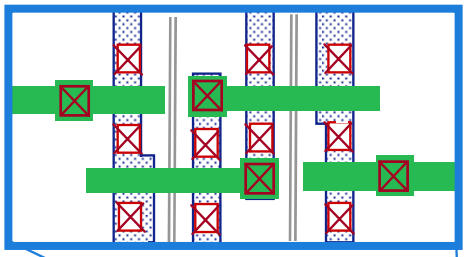
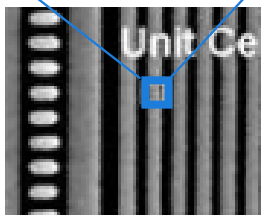
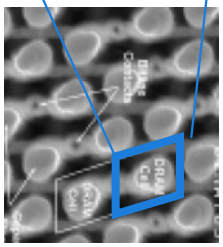
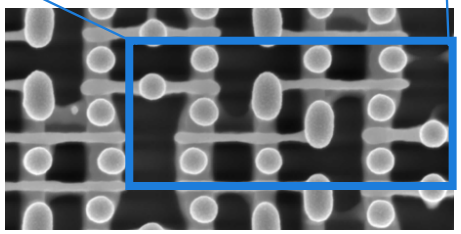
Shrink

- Shrink speed is defined using “half pitch”
- Half pitch is led by Flash with k factors below 0.30
- DRAM is trailing Flash by about 10%
- Logic and µP are trailing Flash by about 50%
- Logic customers use “node” instead of “half pitch”
- On average, the relation is 70% “half pitch” = ”node”

IC characteristics & Lithography implications

	NAND Flash	DRAM	Logic / SRAM
Cell layout			
Typical Device Pattern			
Device:	X-point storage transistor	Transistor + Capacitor	6 Transistor (SRAM)
Typical Cell Size:	4 F^2	6~8 F^2	50~60 F^2
Bits/cell	1 → 4	1	1
Critical Patterns:	1D	1D & 2D	2D
Critical Pitch:	Dense	Dense	Random
Shrink Challenge:	Resolution	Imaging & overlay	OPC, DoF
RET:	Strong	Moderate	Weak
k_1 limit:	0.27 ~ 0.29	0.29 ~ 0.31	0.36 ~ 0.38

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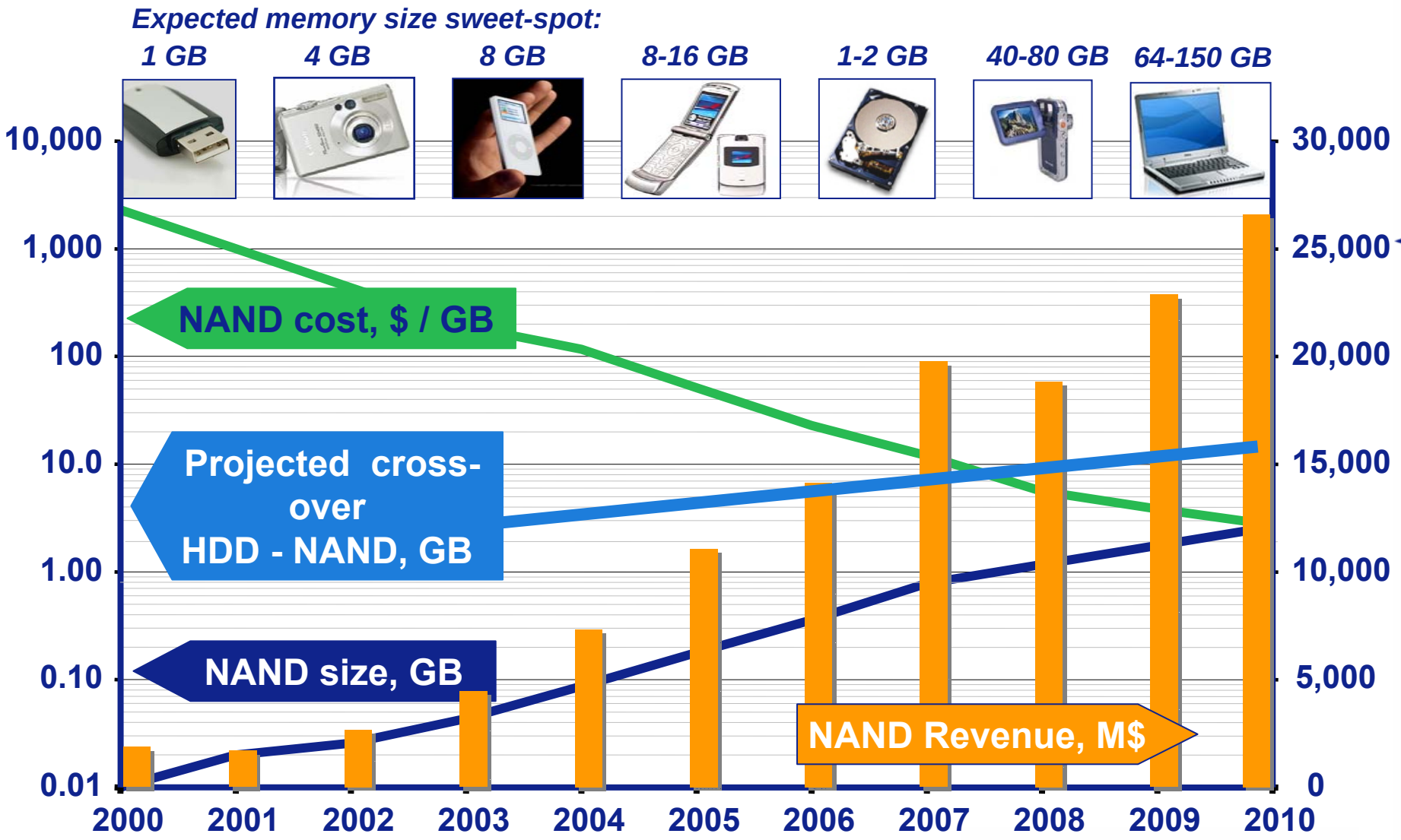
Shrink drives cost per function and market growth



Source: Gartner Dataquest, iSuppli, ASML

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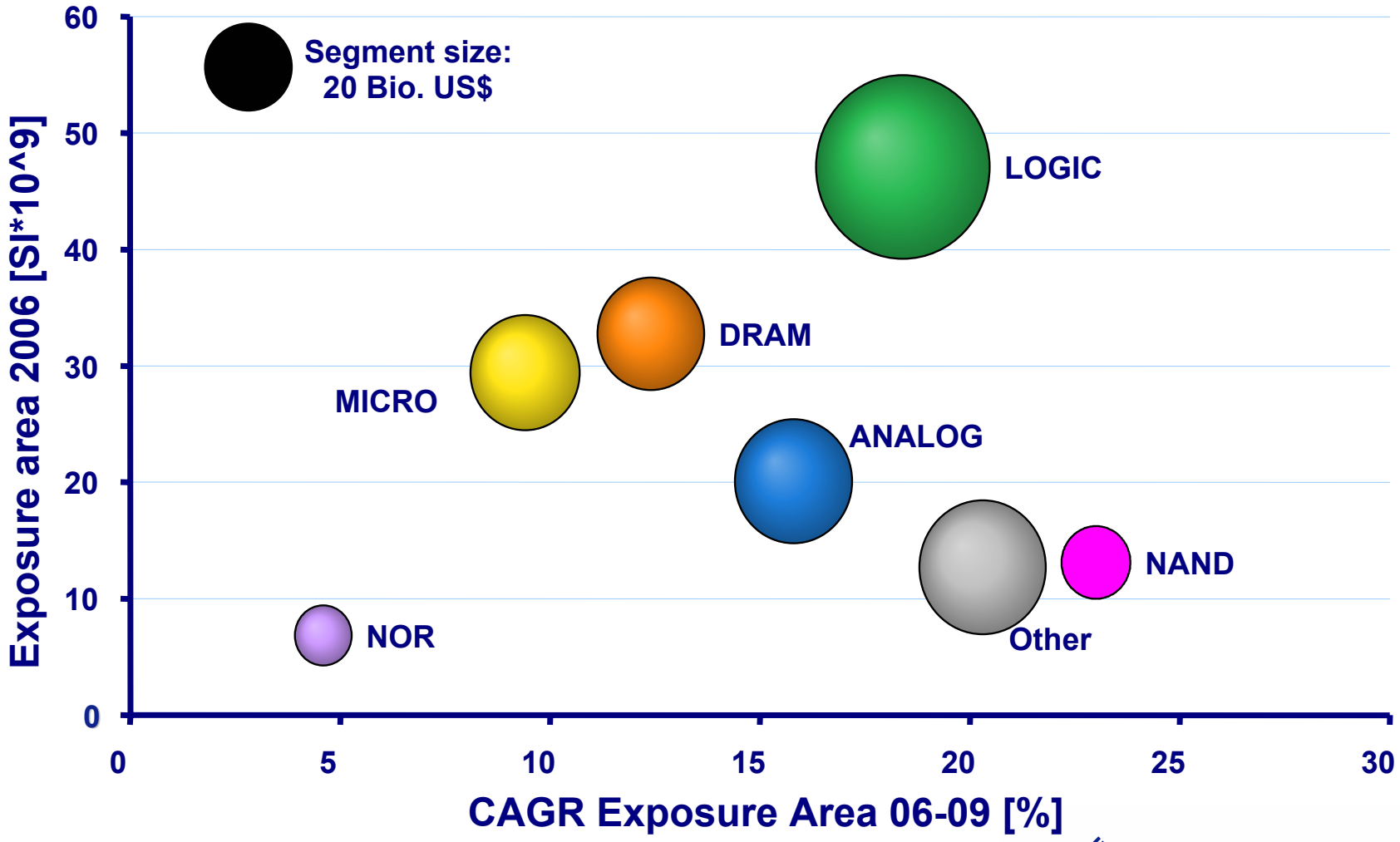
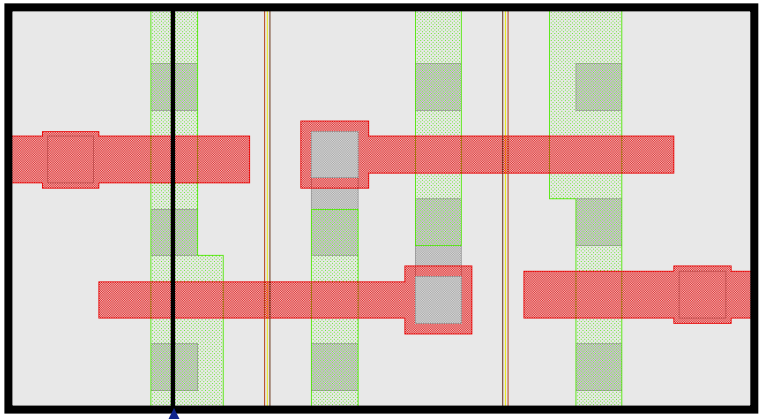
NAND Flash fastest growing IC segment between 2006 and 2009 in terms of silicon exposure area



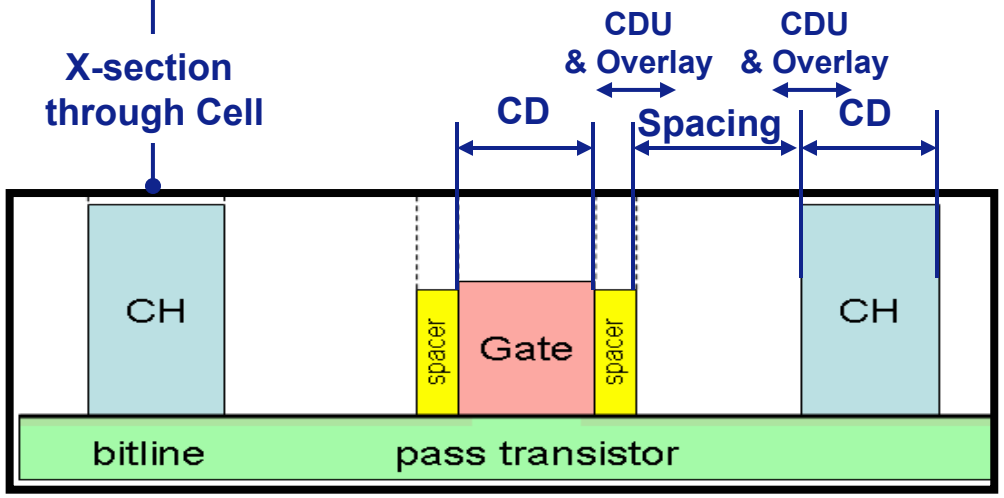
Sources: ASML MCC, VLSI Research, iSuppli, SIA

Resolution, CD uniformity & overlay drive shrink

Layout 6 transistor SRAM Cell



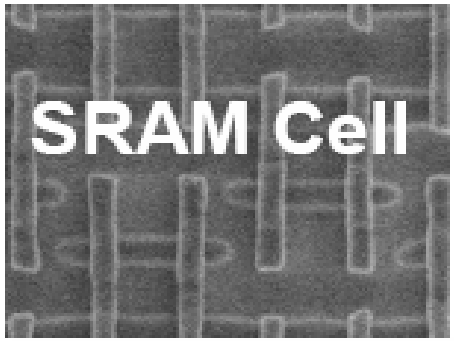
X-section through Cell



Design Rule & Cell Area [μm²]

Node	Aggressive	Typical	Relaxed
130 nm	2.00	2.50	3.00
90 nm	1.00	1.25	1.50
65 nm	0.45	0.55	0.80
45 nm	0.20	0.27	0.34
32 nm	0.10	0.13	0.19

cell area 0.24 μm2
metal pitch 130nm
ArF immersion



Source: IMEC, TI

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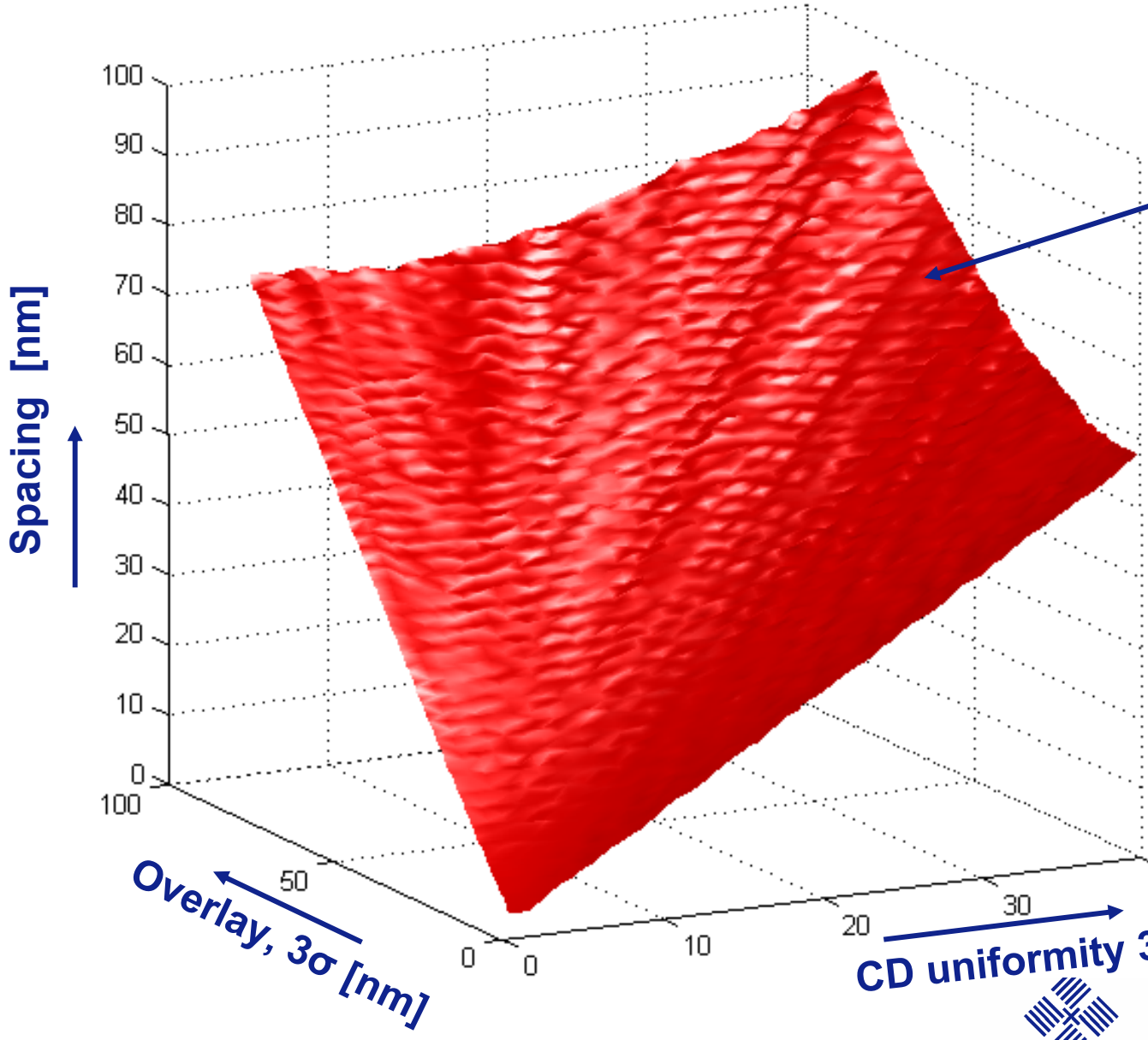
Overlay and resolution (-control) key for device scaling



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Content

- The demand for shrink continues
- Litho roadmap
  - Dry
  - Immersion
  - Double patterning
  - EUV
- Litho integration
- Litho cost
- Summary

Roadmap scenarios

Resulting k_1 as function of resolution, wavelength and NA

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

k_1 = (half pitch) * NA / wavelength

Most aggressive k_1 in production today = 0.3,
physical limit single exposure = 0.25
Practical limit double patterning = 0.2

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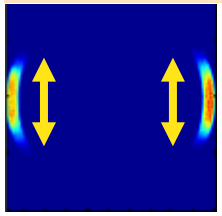
First super high NA immersion system enables 45 nm

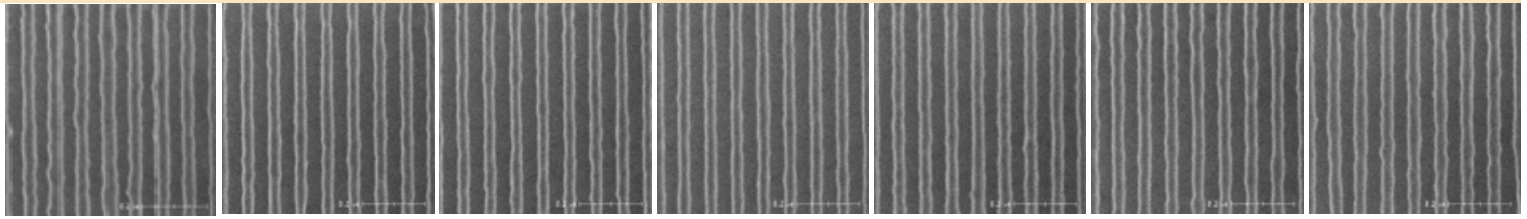
	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

First super high NA immersion system enables 45 nm

Overview dense line 1700i imaging results

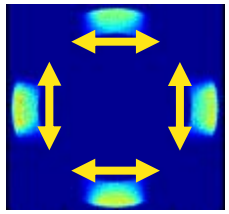
42nm 1.2NA, σ=0.89/0.98, Dipole X-35, Y polarization, k1 =0.261

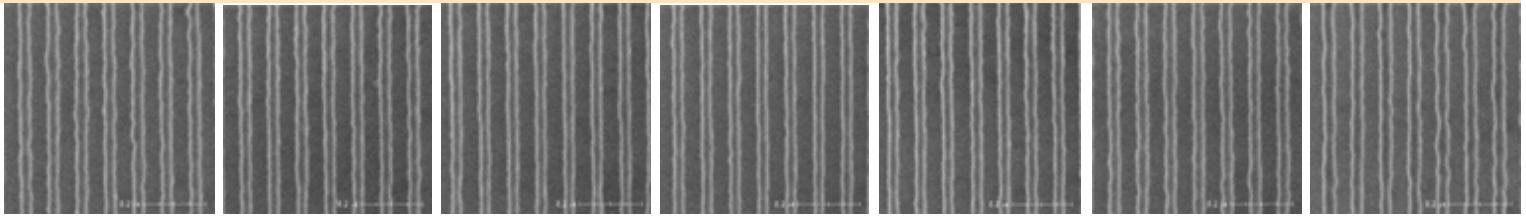




950nm DoF -500nm -300nm -180nm NF +180nm +300nm +450nm

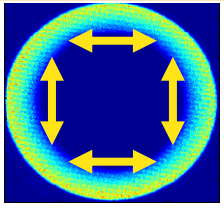
45nm 1.2NA, σ=0.82/0.97, C-Quad-30, XY polarization, k1 = 0.28

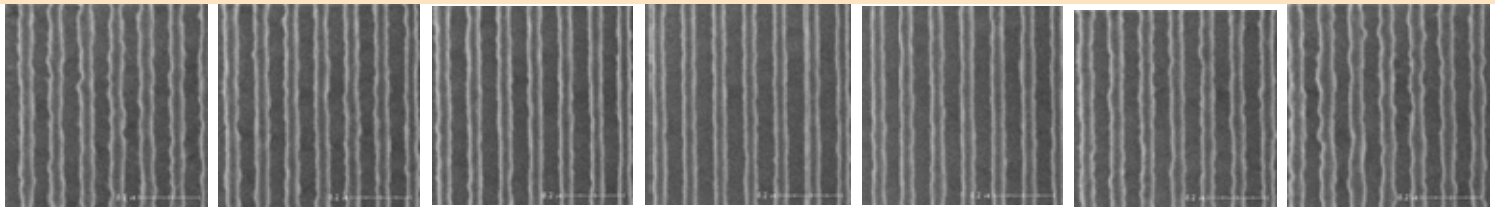




500nm DoF -300nm -240nm -120nm NF +60nm +120nm +210nm

50nm 1.2NA, σ=0.74/0.94, annular, XY polarization, k1 = 0.31





400nm DoF -210nm -150nm -90nm NF +90nm +150nm +210nm

@ 550mm/s Scan speed

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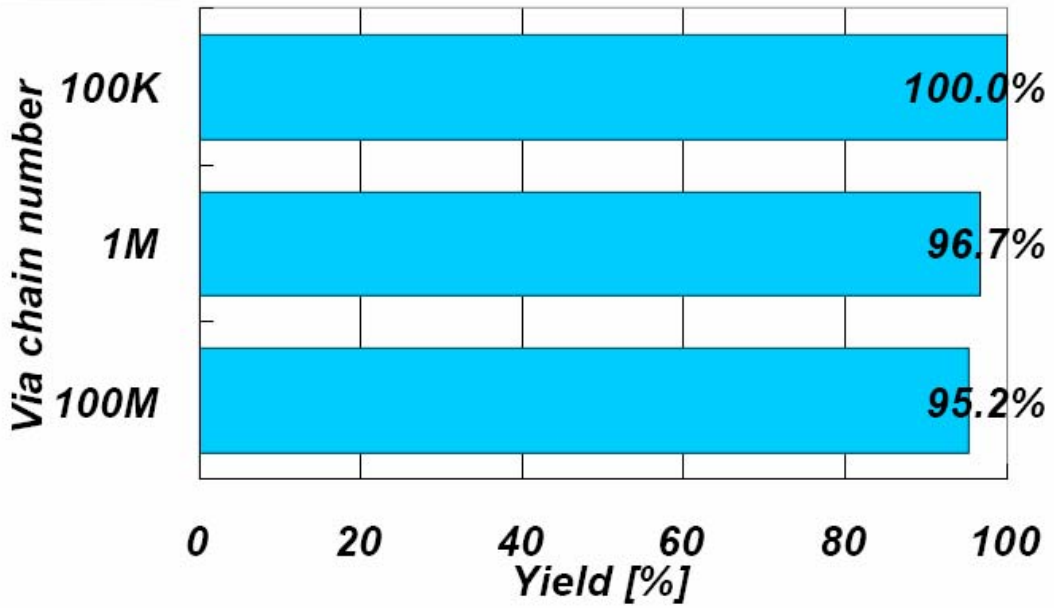
Immersion performance deficiency not impacting yield

Via chain yield for 55-nm devices

NEC

Metal1-via-metal2; all wet-tool NA=0.93



Immersion lithography does not degrade the yield of the device.

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Teruhiko Kodama, NEC, Symposium on Immersion Technology, Kyoto, oct 06

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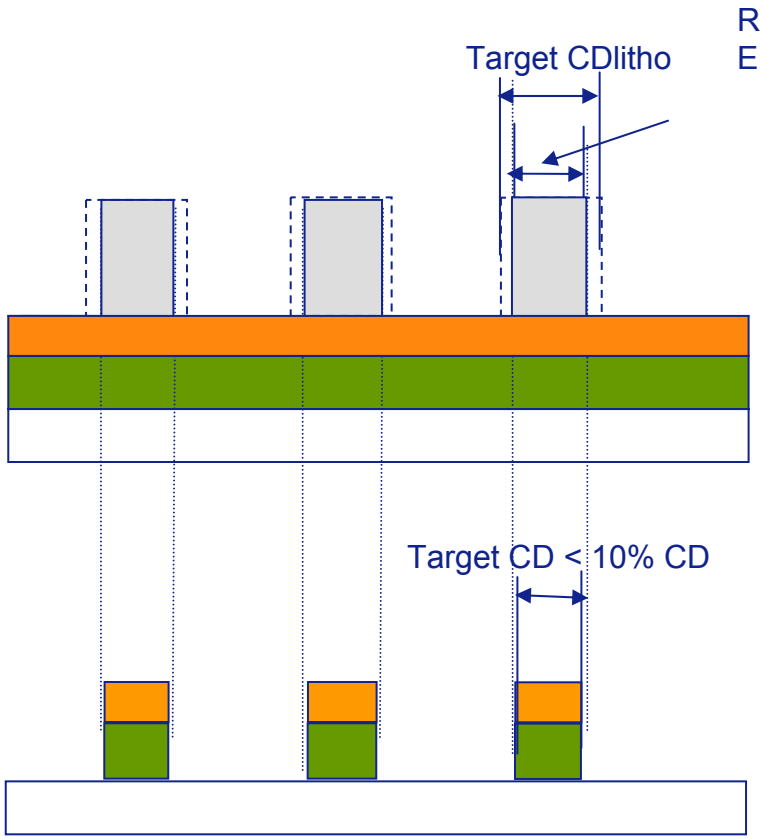
Roadmap scenarios, the impact of immersion

Water-based 193 not sufficient for 32-nm half pitch

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

Max NA water-based 193 nm immersion requires double patterning to get to 32 nm

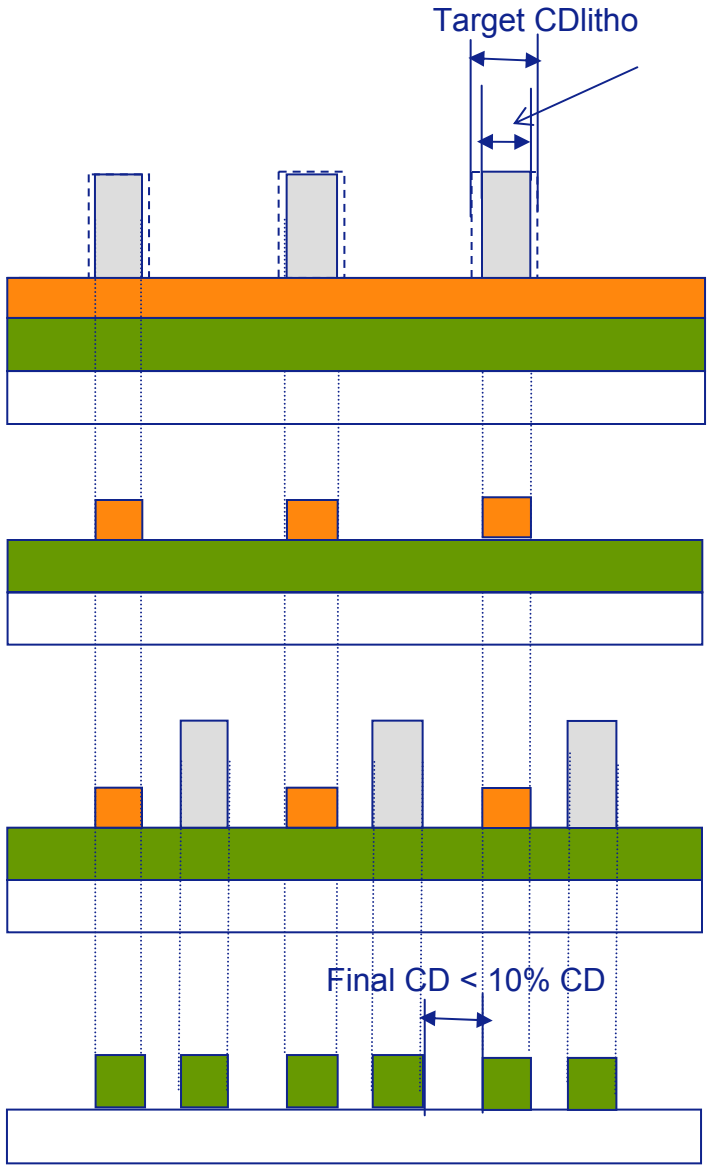
Single Exposure (like EUV) Litho requirements



CD determined by 2 error components litho and etch:

ΔCDlitho < 7% of CD
Overlay < 20% of CD

Litho Double Patterning Litho requirements



Real CDlitho is smaller than target CDlitho
Error caused by litho

CD determined by 8 error components; 2 x litho, 2 x etch and overlay:

ΔCDlitho < 3,5% of CD
Overlay < 7% of CD

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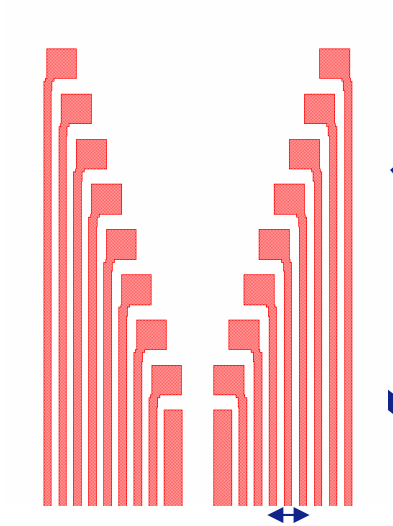
Double line patterning; 32-nm half pitch Flash

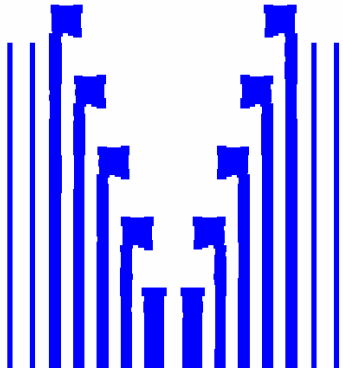
Target
Min Pitch 64nm
k1 = 0.20

SPLIT + OPC

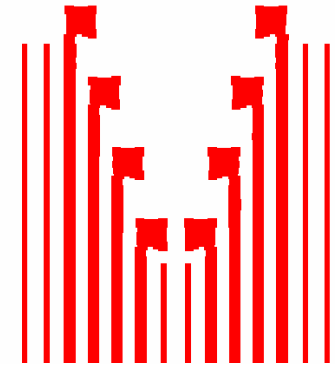
Poly patterning
Annular 0.8/0.5, X-Y polarized
XT:1700i, 193nm - 1.2NA

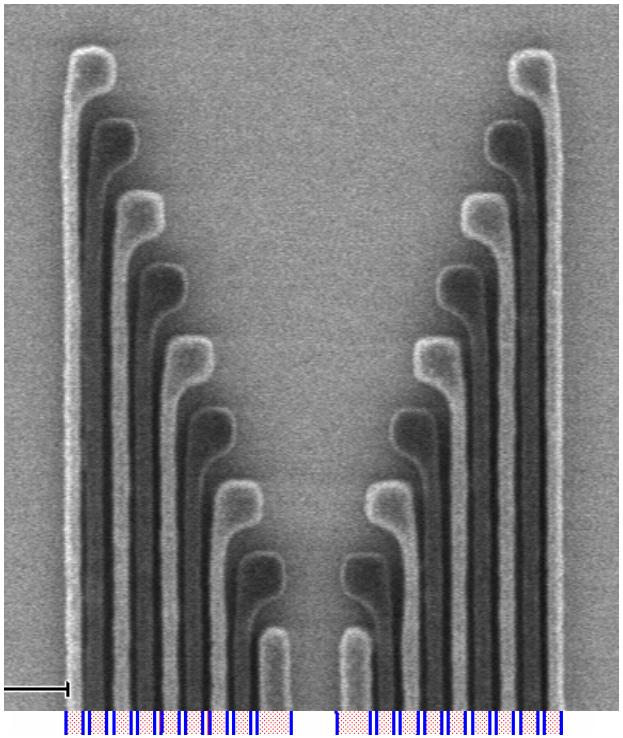


MASK A

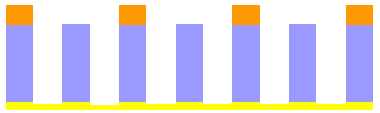


MASK B





Hard mask
Poly



Co work ASML, Imec, Synopsys and Mentor Graphics

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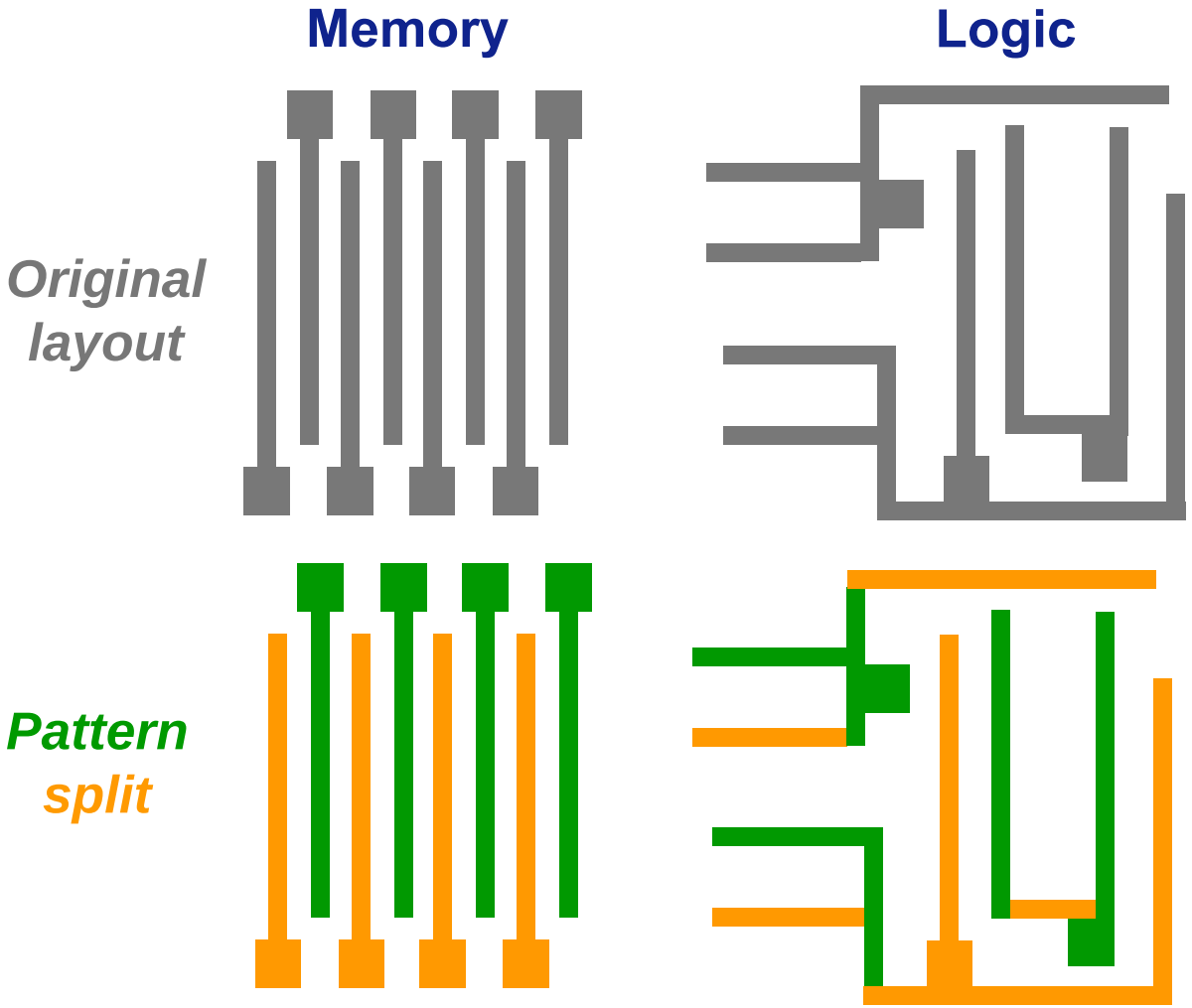
New software & algorithms required to split & optimize OPC and stitching for Double Patterning



Challenges

- Correct decomposition
- OPC for decomposition
- Model-based stitching error compensation

Increasing Difficulty

- NAND Flash
- DRAM
- Restricted Logic
- Random Logic

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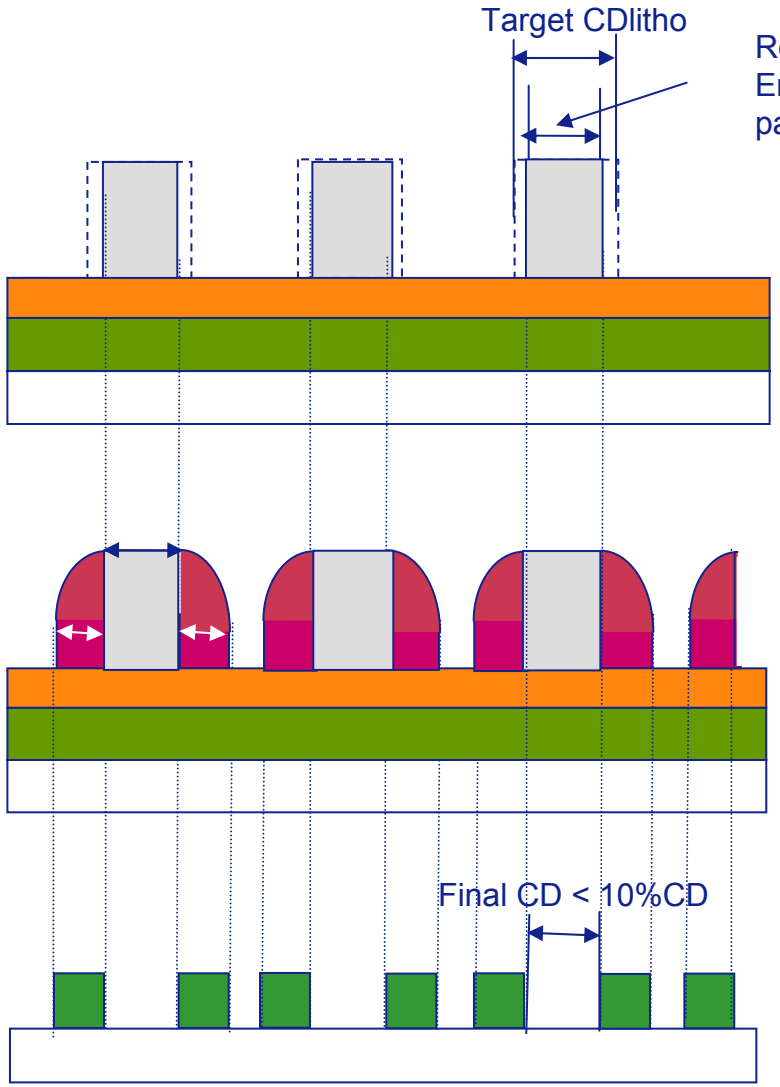
Spacer Double Patterning Litho requirements



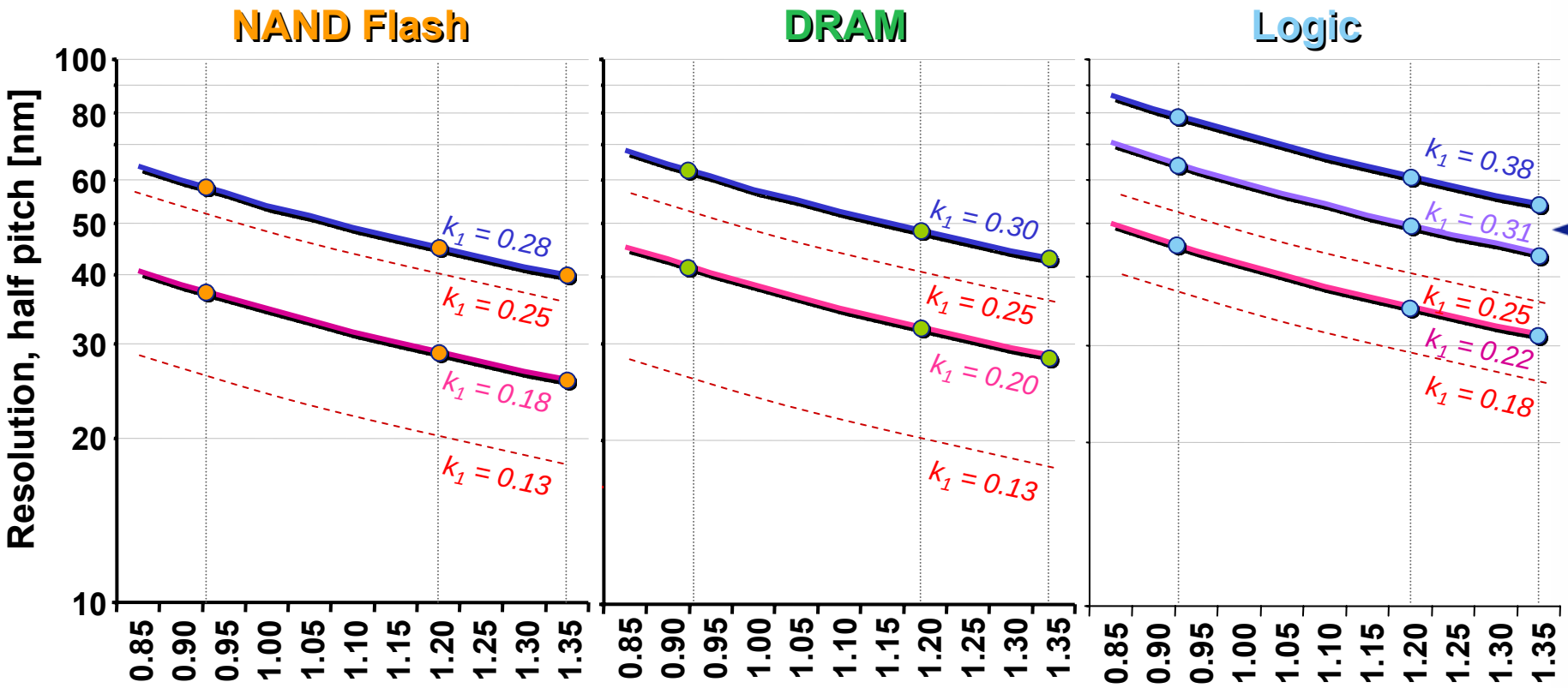
CD determined by 11 error components; litho, etch, spacer deposition, trim and final etch:

ΔCDlitho < 3 % of CD
Overlay < 20% of CD

CD and overlay litho budget challenge

Litho exposure Equipment parameter as percentage of CD	Single exposure	Litho double patterning	Spacer double patterning
ΔCD	7%	3,5%	3%
Overlay	20%	7%	20%
# mask steps	1	2	2-3
# process steps relative to single exposure	1	2	3-4

Lithography Limits for ArF Single & Double Patterning



Single Exposure limit

Double Exposure limit

Double Patterning limit

Physical limit

ArF	NAND		DRAM		Logic		
NA	SE	DPT	SE	DPT	SE	DE	DPT
0.93	58	37	62	42	80	65	45
1.20	45	29	48	32	60	50	35
1.35	40	26	43	29	55	45	31

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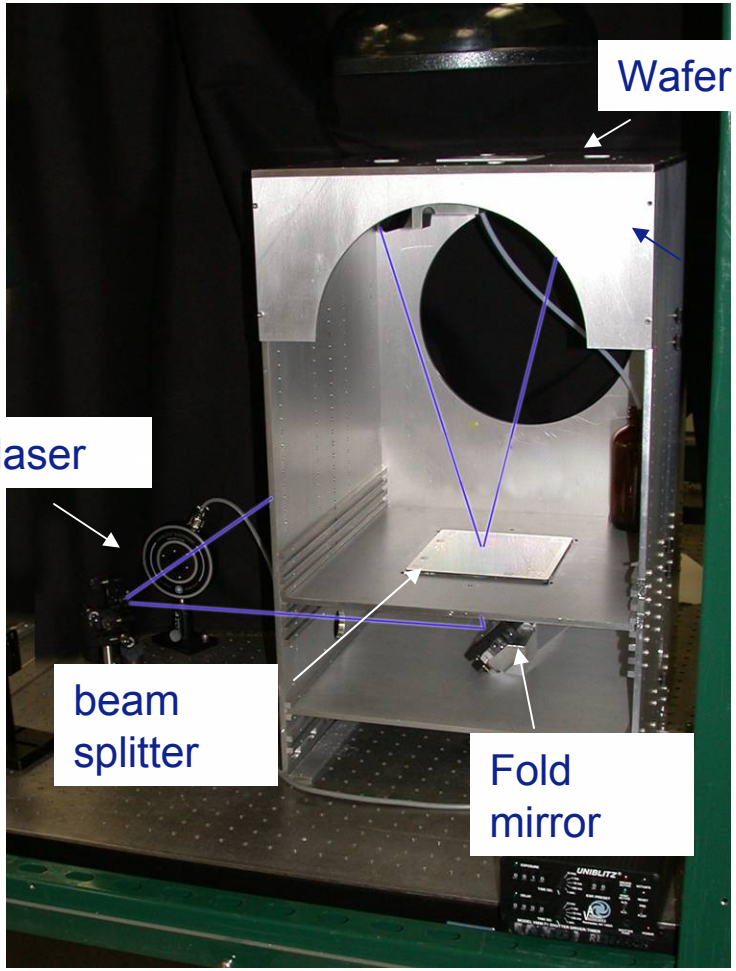
32 nm half pitch with 193 immersion extremely challenging

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20		0.40	0.28				
	1.35			0.31	0.22	0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

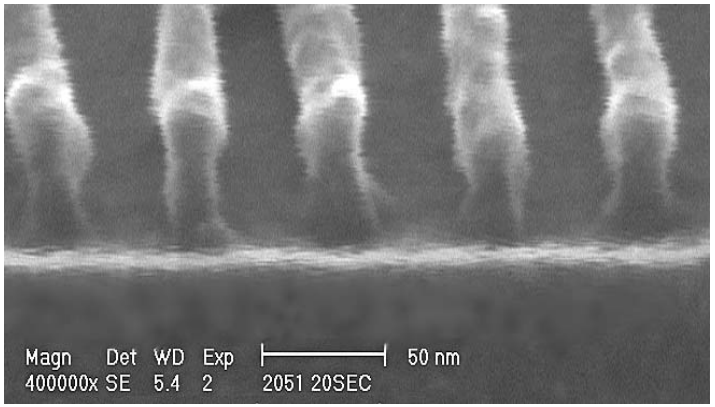
NA 1.55 requires new liquid, new glass and very low k1 to extend to 32nm

29-nm imaging on interference set-up

Version I Interferometer



Imaging results with Dupont IF169



85 nm ARC-29A, 50 nm PARIM850 resist

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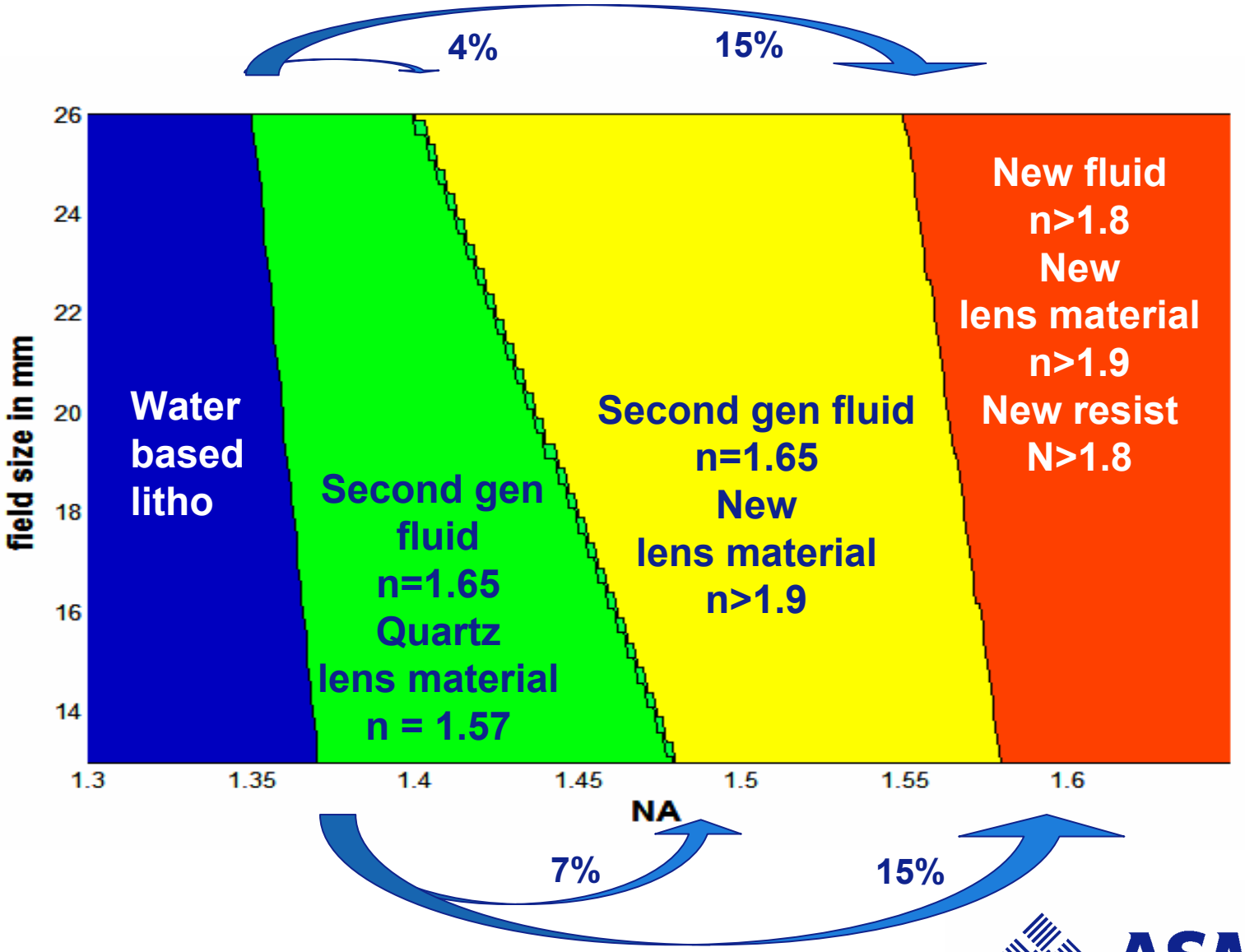
Apertures, field sizes and refractive indices



Historic reduction stepper imaging technology changes

Technology	Incubation time [yr]	Production Insertion	Diffraction limit [nm]	Incremental Improvement %
436 nm/air	-	1980	109	-
365 nm/air	3	1989	91	19
248 nm/air	9	1995	62	47
193 nm/air	7	2002	48	28
157 nm/air	Failed	-	39	23
193 nm/water	3	2006	34	44
193 nm/HI	> 6	>2010	29	15
13 nm/ vacuum	>10	>2010	3.3	1031

EUV the only high volume opportunity

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
	1.20							
	1.35					0.15		
	1.55				0.26	0.18		
13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

EUV required for 32 nm as cost reduction for double patterning and more extendable technology than non water immersion

Installation of EUV in progress (Dec. 2006)

Leuven

Albany

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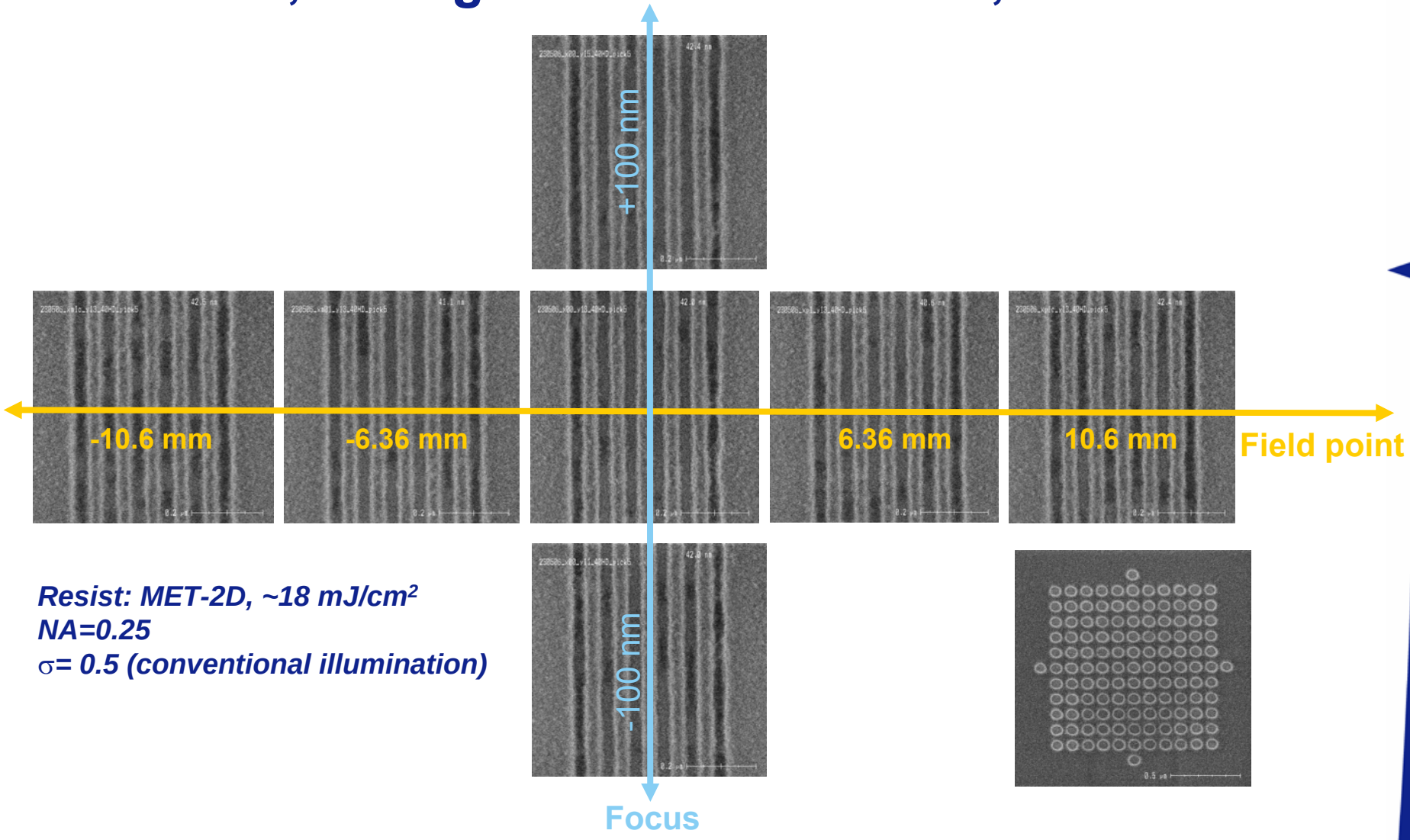
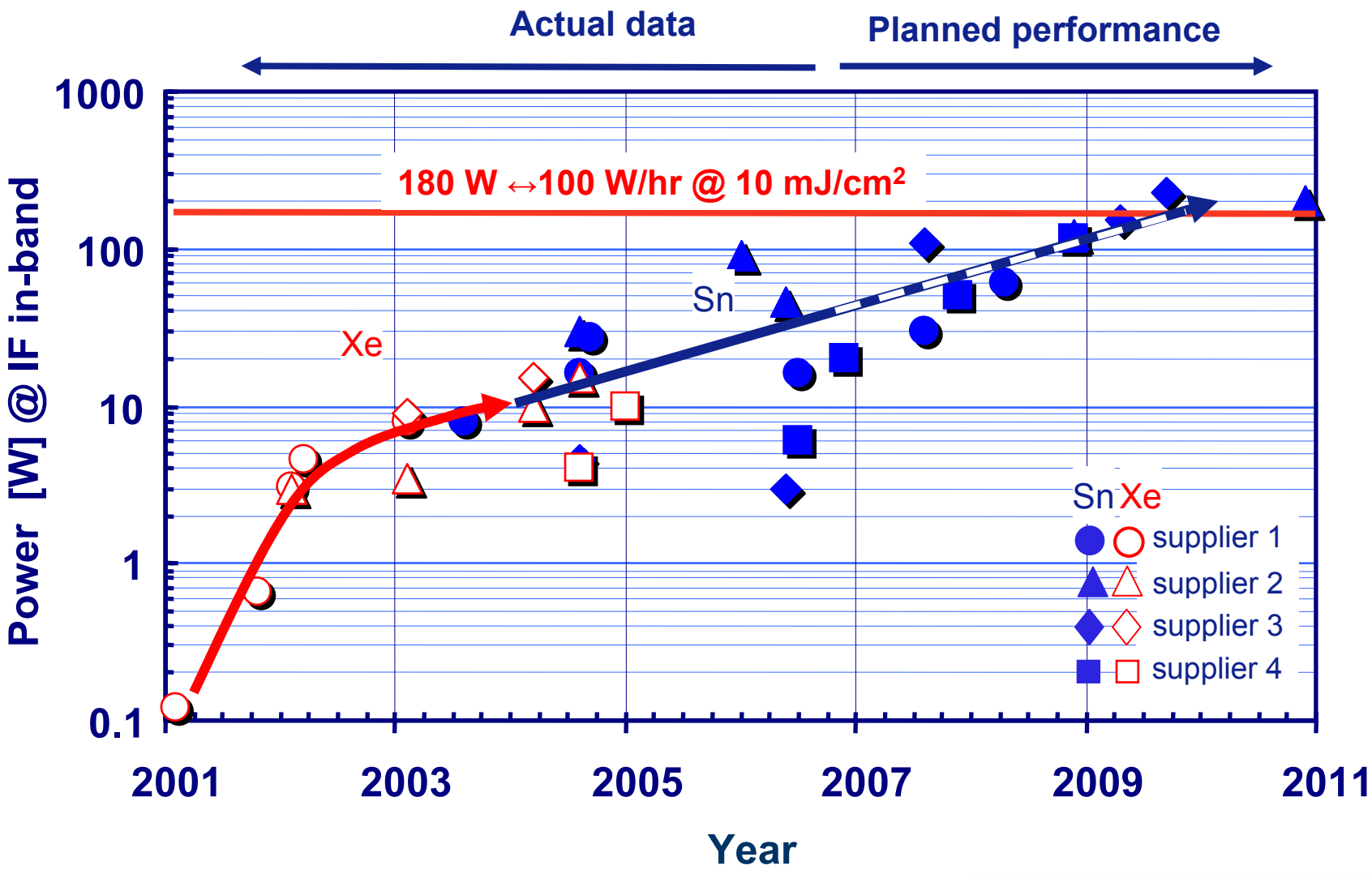
Full field, through focus 40 nm lines, 55 contacts



Resist: MET-2D, ~18 mJ/cm²
NA=0.25
σ= 0.5 (conventional illumination)

Source power progress has been increasing



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Likely technology roadmap

	half pitch	100	65	45	32	22	16	11
	year		2005	2007	2009	2011	2013	2015
λ [nm]	NA							
248	0.80	0.32						
193	0.93		0.31					
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13.5	0.25				0.59	0.41		
	0.35					0.57	0.41	
	0.45						0.53	0.37

Pitch relaxation or Double patterning

Low k_1 challenge

Fluid/ material challenge

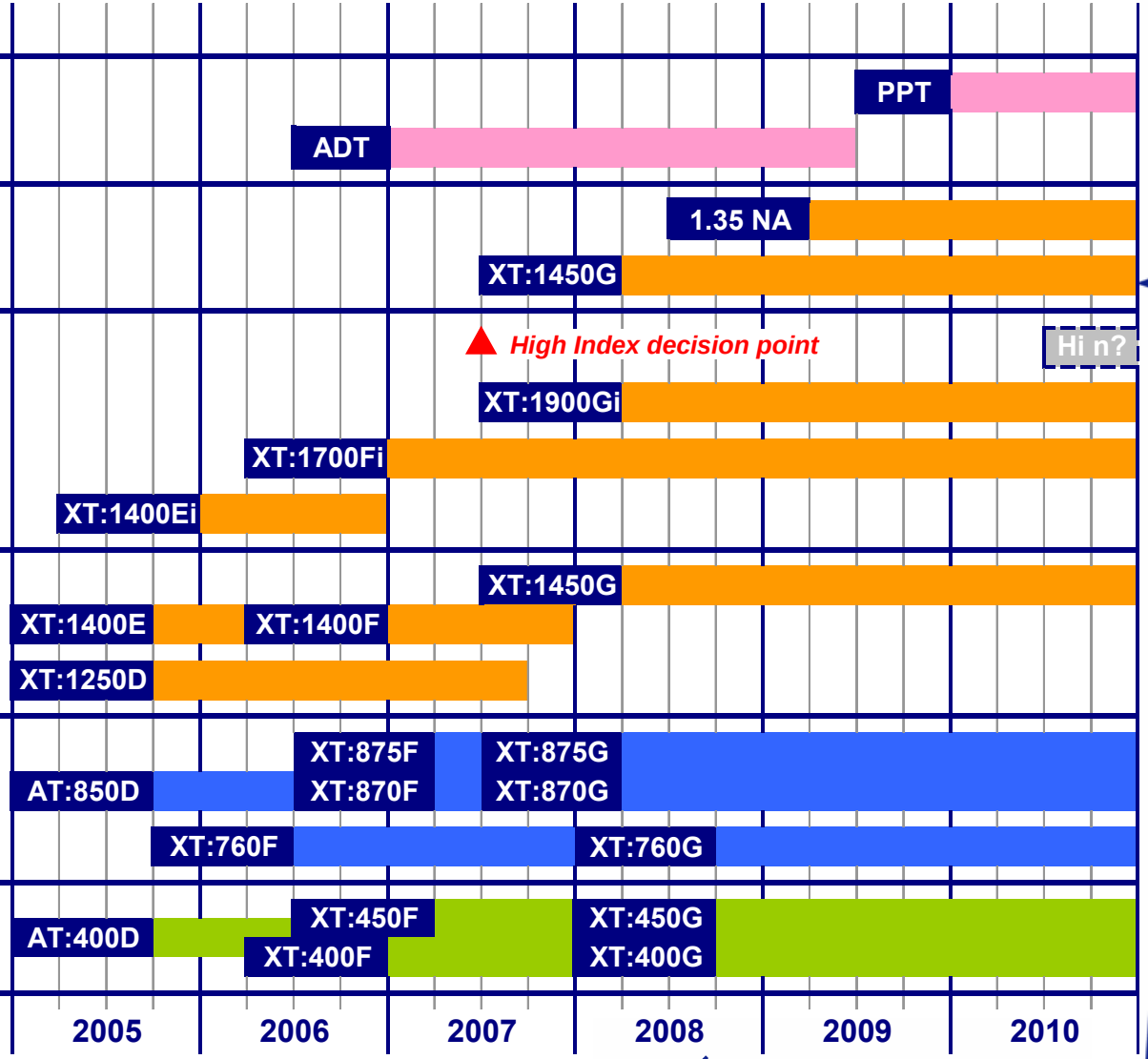
Infrastructure challenge

likely

opportunity

ASML 300mm Product Roadmap

Technology	Resolution	NA	Overlay
EUV 13 nm	32 nm	0.25	4nm
	40 nm	0.25	12nm
Double Patterning	< 30 nm	1.35	<4nm
	< 40 nm	0.93	4nm
Immersion 193 nm	< 40 nm	> 1.5	
	40 nm	1.35	6nm
	45 nm	1.20	7nm
	65 nm	0.93	12 nm
ArF 193nm	57 nm	0.93	6 nm
	65 nm		8 nm
	70 nm	0.85	8 nm
KrF 248 nm	90 nm	0.80	8 nm
	110 nm		12 nm
	130 nm	0.70	12 nm
i-Line 365 nm	220 nm	0.65	12nm
	350 nm		15nm



ASML

Content

- The demand for shrink continues
- Litho roadmap
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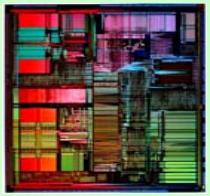
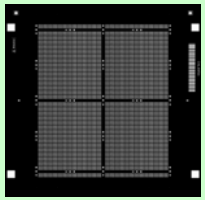
High k_1 : Low Design to Wafer Integration

High k_1 (>0.5) : Independent Design, Mask Manufacture & Wafer Processing

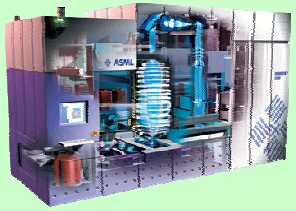
Design & Layout



Mask Shop



Wafer Fab



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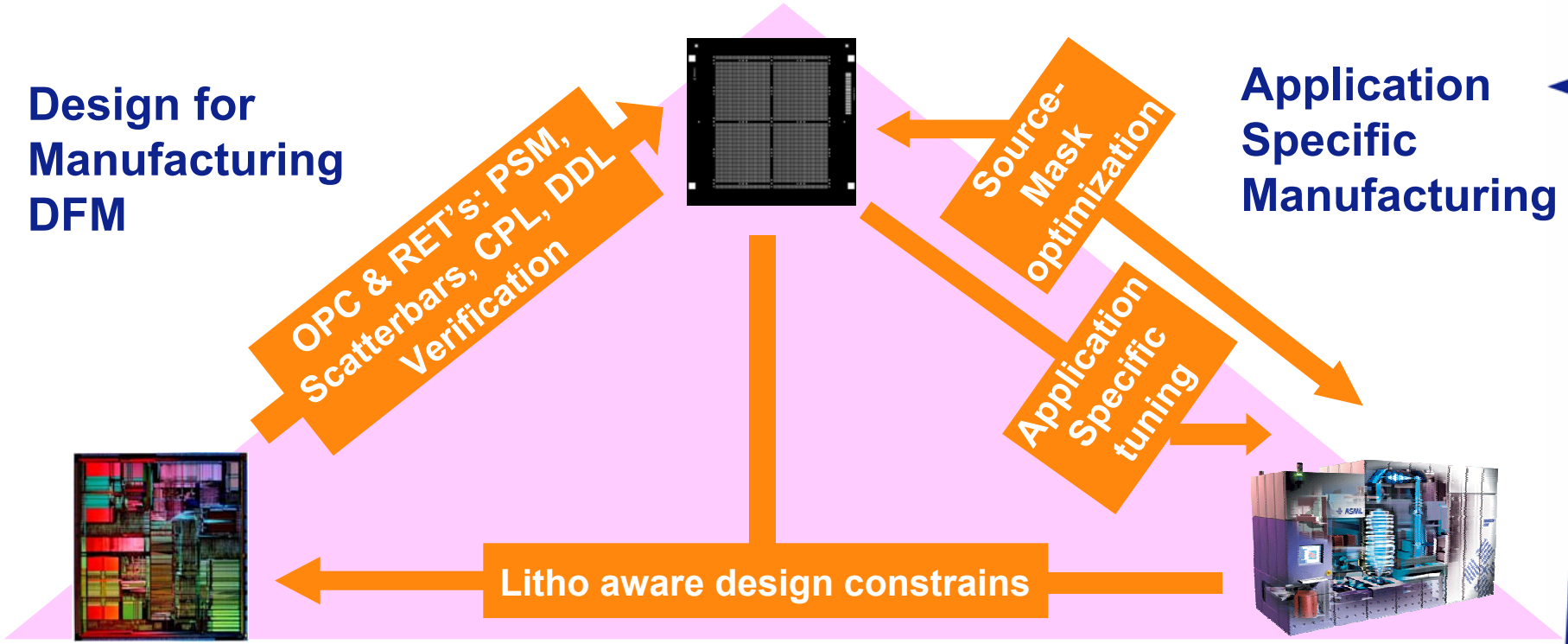
Low k_1 : High Design to Wafer Integration

Low k1 (<0.4) : Integration of design, mask and Lithography processes



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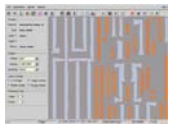
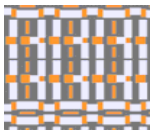
ASML & Brion: Integrated manufacturing solution

ASML MaskTools

Reticle Enhancement Technologies

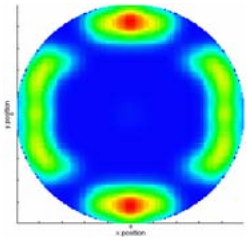


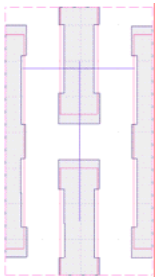
Scattering Bars placement technology



Chrome-less Phase-shift technology (CPL)

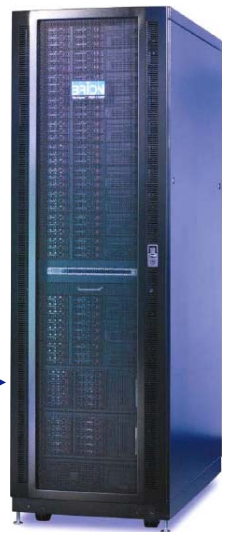
LithoCruiser: Source & Mask Optimization



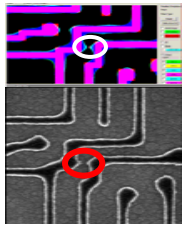


Brion

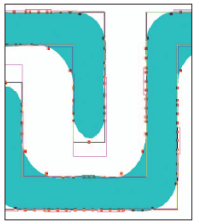
Ultra fast verification & RET/OPC



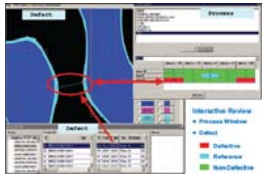
Tachyon Platform



Production Litho Verification



Production RET/OPC



Process Window Coverage

Source definition

Scanner data & optimization

ASML TWINSCAN

Highest productivity scanner

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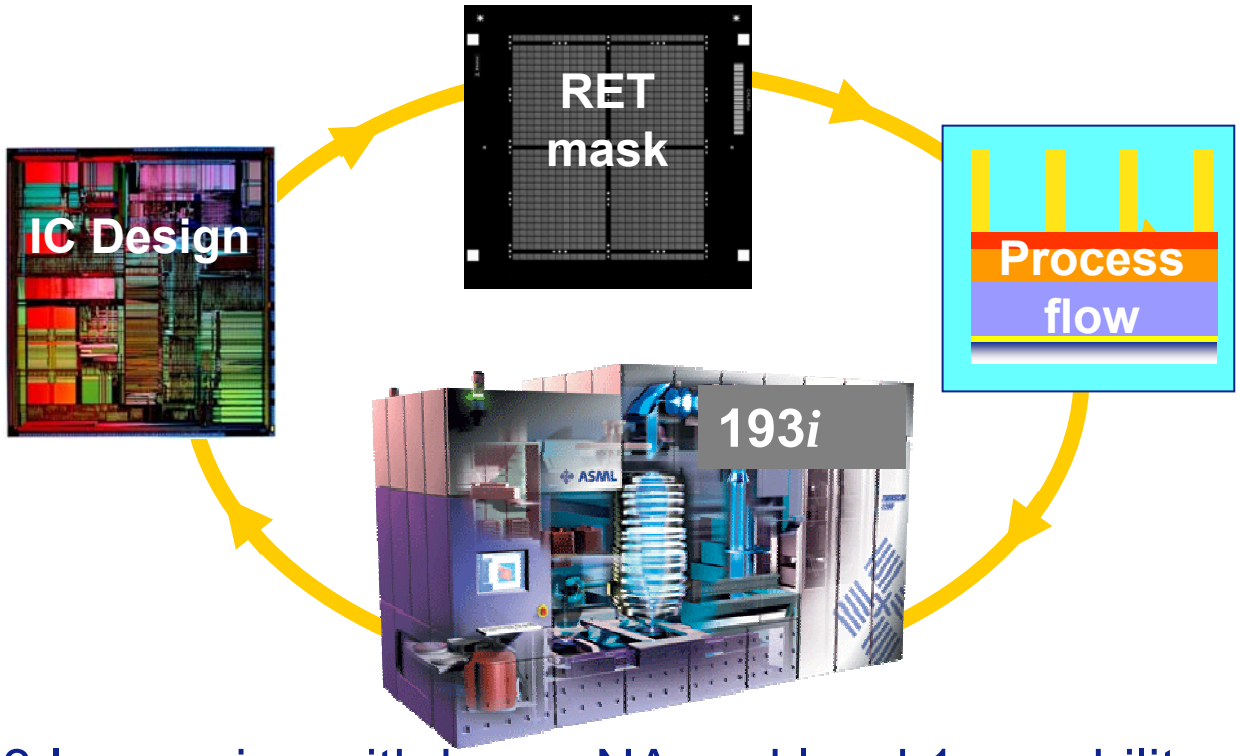
Extending Lithography is driving Integration of Design, Mask, Process and Exposure



- 193 Immersion with hyper NA and low k1 capability
- IC design for manufacturability, DFM
- Source-mask optimization, Litho, RET&OPC
- Process flow optimized for low contrast imaging, optimal CD and stitching (overlay)

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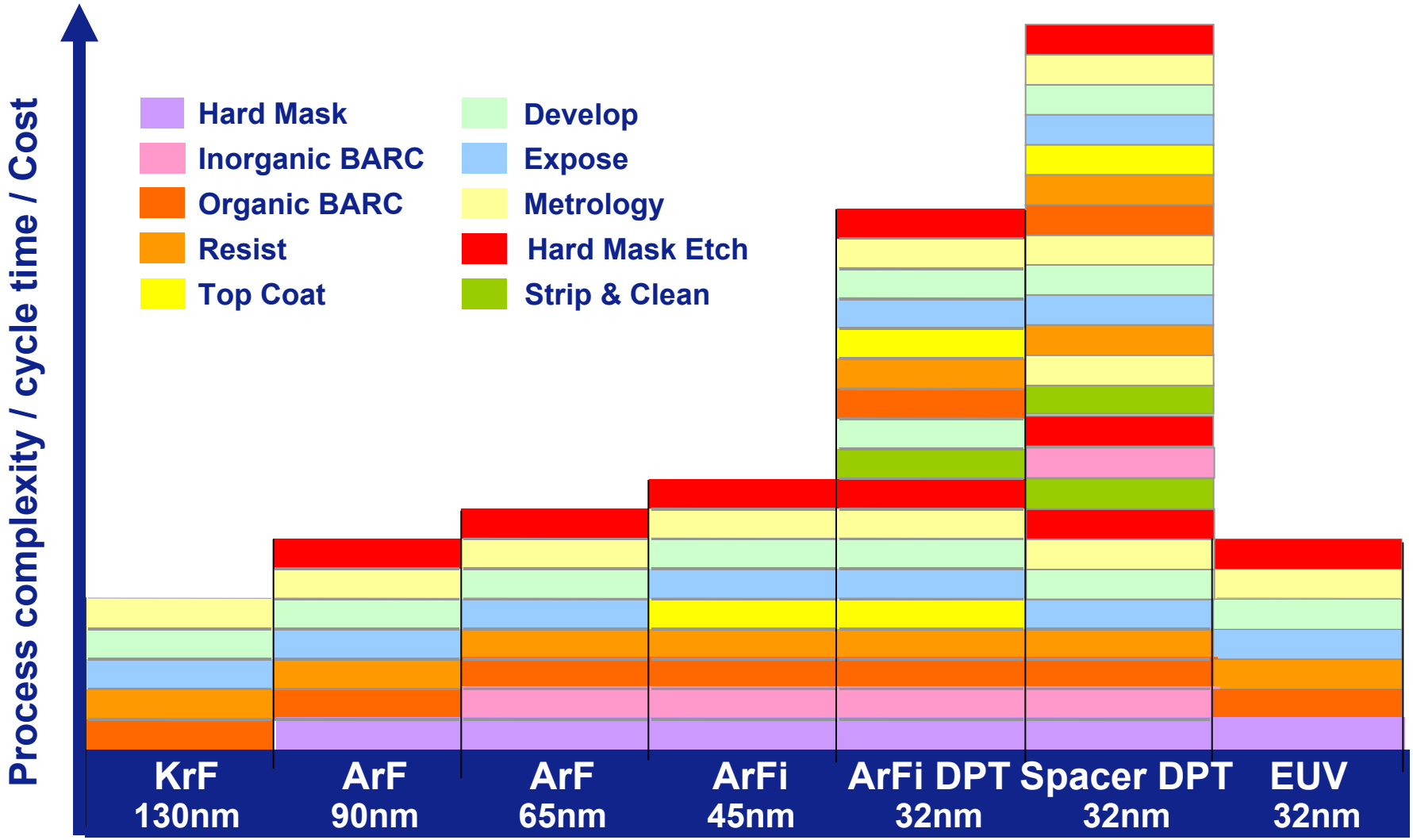
Increased litho process complexity drives cost



DPT = Double Patterning

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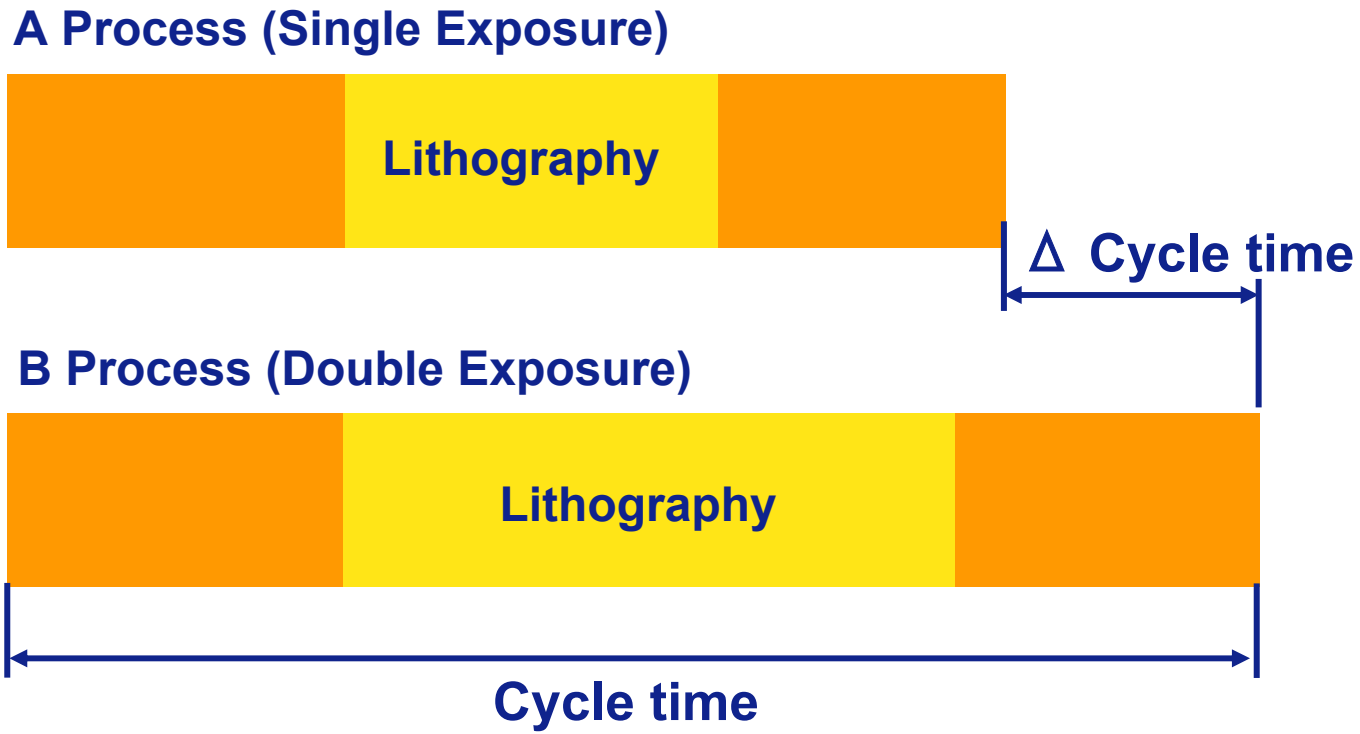
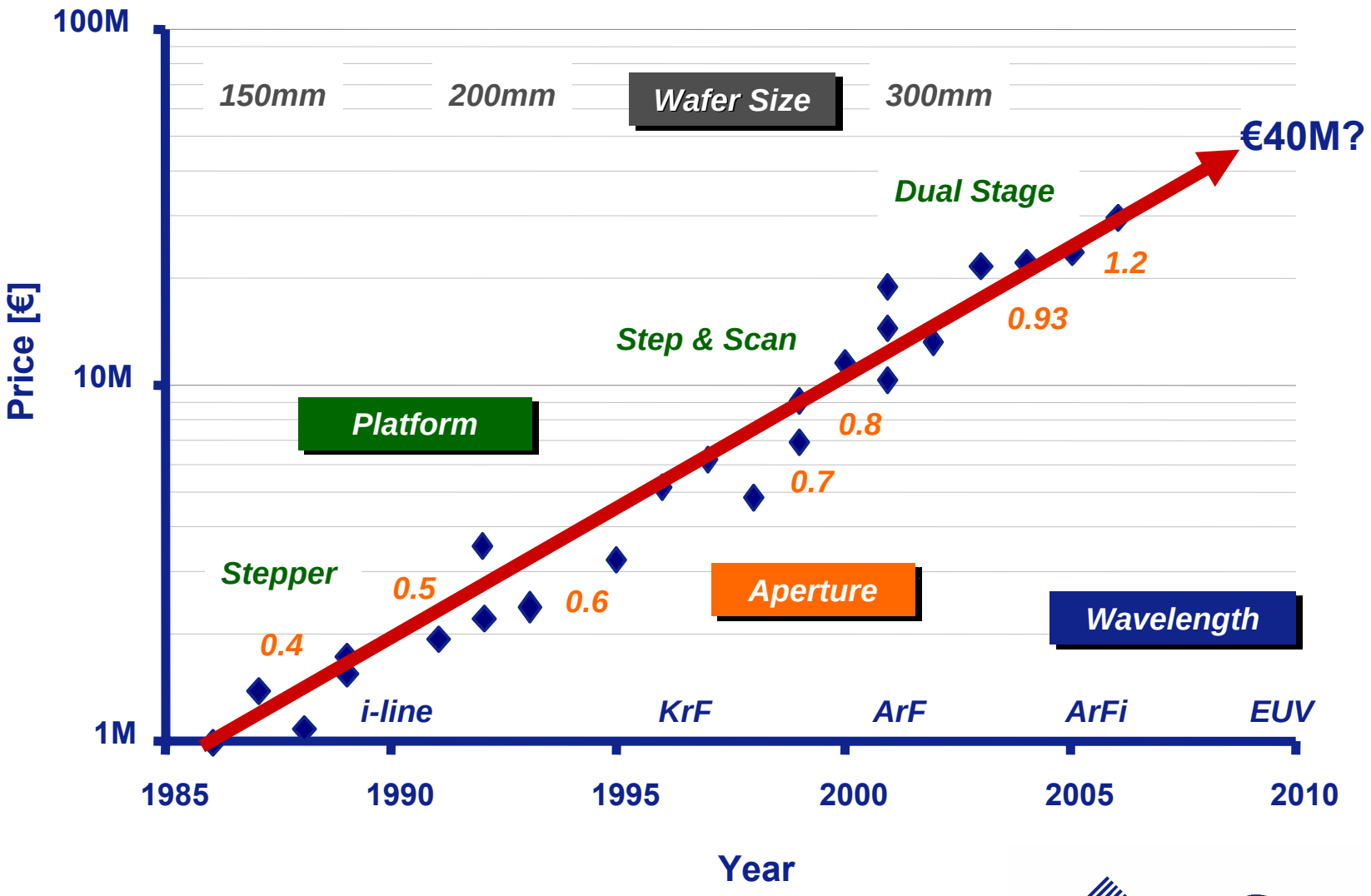
Cycle time of multiple exposure strategies increases



Higashiki, Tosiba, Santa Clara, SPIE march 06

Lithography System Price Evolution



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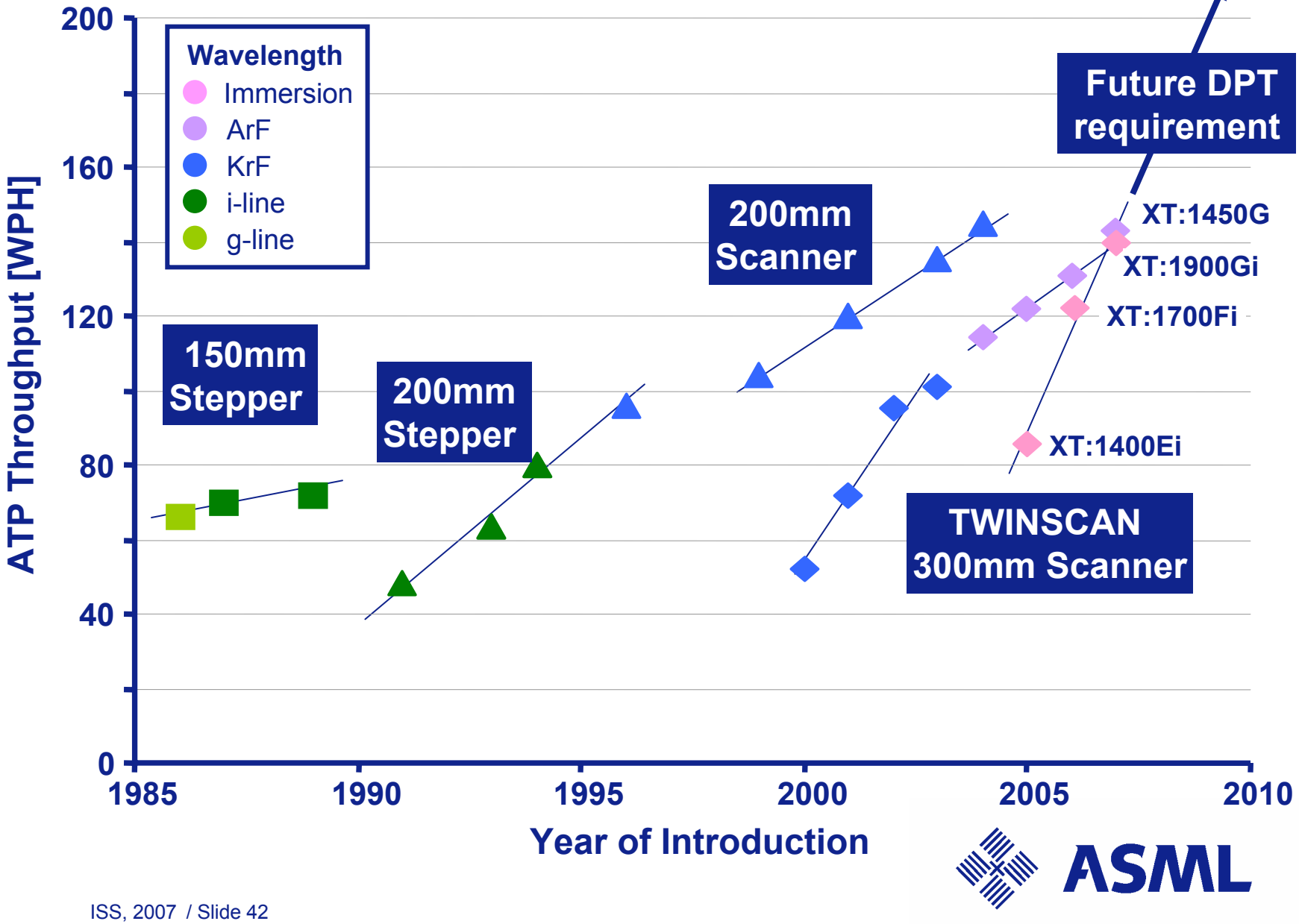
ASML System Throughput Improvement



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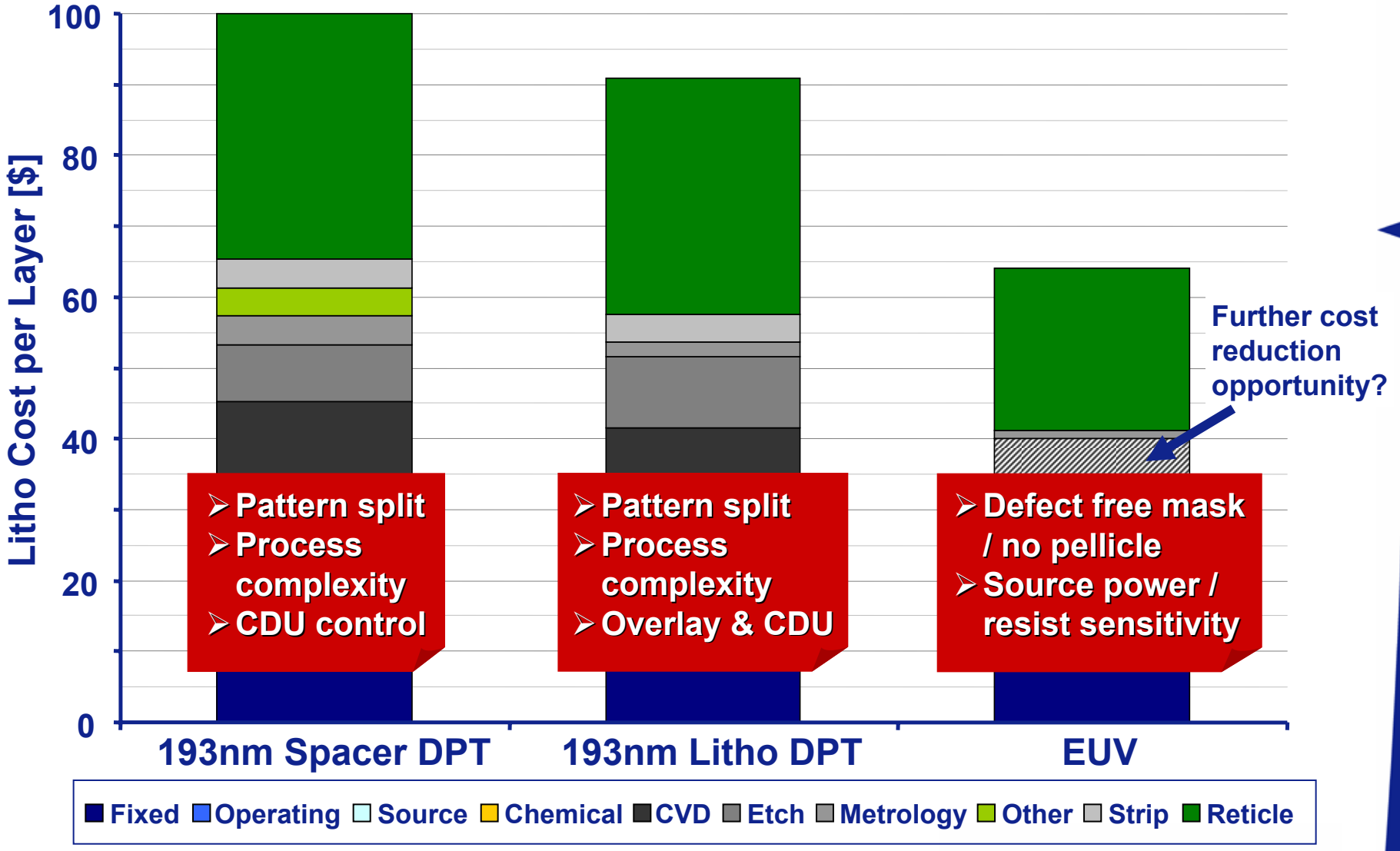
Litho cost per layer: estimates for 32nm

Challenges



** Mask cost based on 5000 wafers / mask usage*

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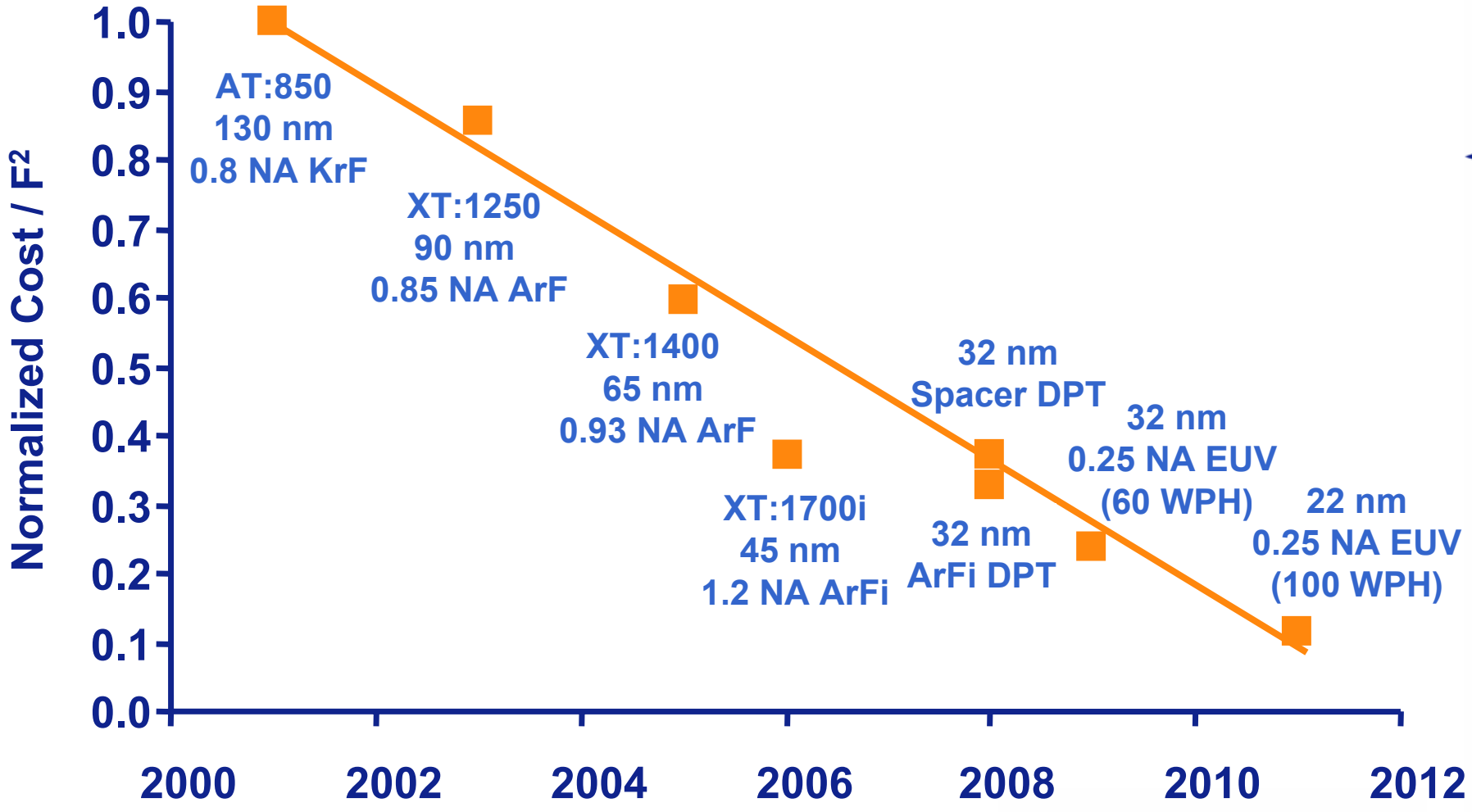
Lithography cost affordability:
Cost per minimum Feature^2 continuous shrink



Source: ASML

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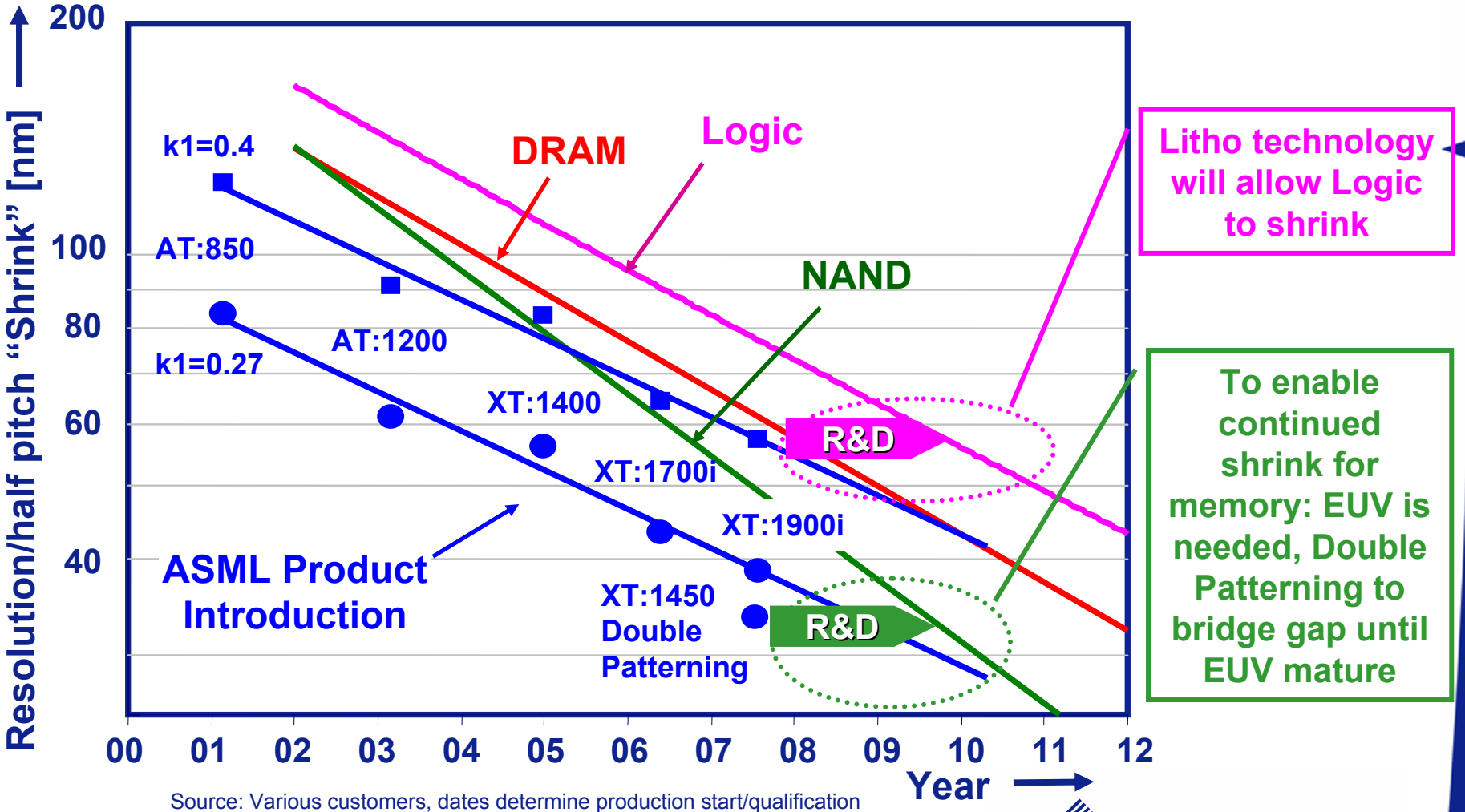
Shrink rates for Logic, DRAM, and NAND flash versus tool introduction at k_1 0.27 and 0.40



Source: Various customers, dates determine production start/qualification

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Summary lithography roadmap

- Water based immersion will capture the 40 nm half pitch using 1.35 NA 193 nm lithography.
- Non water based immersion needs new lens materials to increase resolution capability significantly:
  - New fluid technology advantage for full field resolution limited by existing lens materials to 4%, not sufficient to give economic return to equipment supplier and its user.
  - New lens material technology still needs to mature, this will push any product implementation beyond 2009.
- EUV technology acceptance is significantly growing with shipments of EUV Alpha Demo Tools and orders for pre-production tools but is still below industry threshold.
- Hence double patterning is the only option in the 2008-2009 time frame. ASML will support this with sufficient overlay and productivity on their products in time.

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Summary lithography integration and cost

- Extension of 193 nm is requiring tighter CD and overlay, yielding DPT split and processing. This will drive the integration of design, mask, process and exposure, resulting in integrated DFM solutions as well as mask and application specific manufacturing.
- EUV becomes a cost, cycle time and performance improvement opportunity due to more CD and overlay tolerant single patterning process and single mask with low OPC content. However the infrastructure needs to be developed.
- EUV introduction will be driven by the need for shrink from memory manufactures.
- The required amount, performance and complexity of lithography tools, resist, process and mask will go up in any scenario which should be positive for the integral litho business (mask, exposure, process and optimization software tools) however litho cost needs to be addressed by higher productivity.

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Commitment