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Exercises "Electronic Materials"

#9

Exercise 9: Scaling of microprocessors

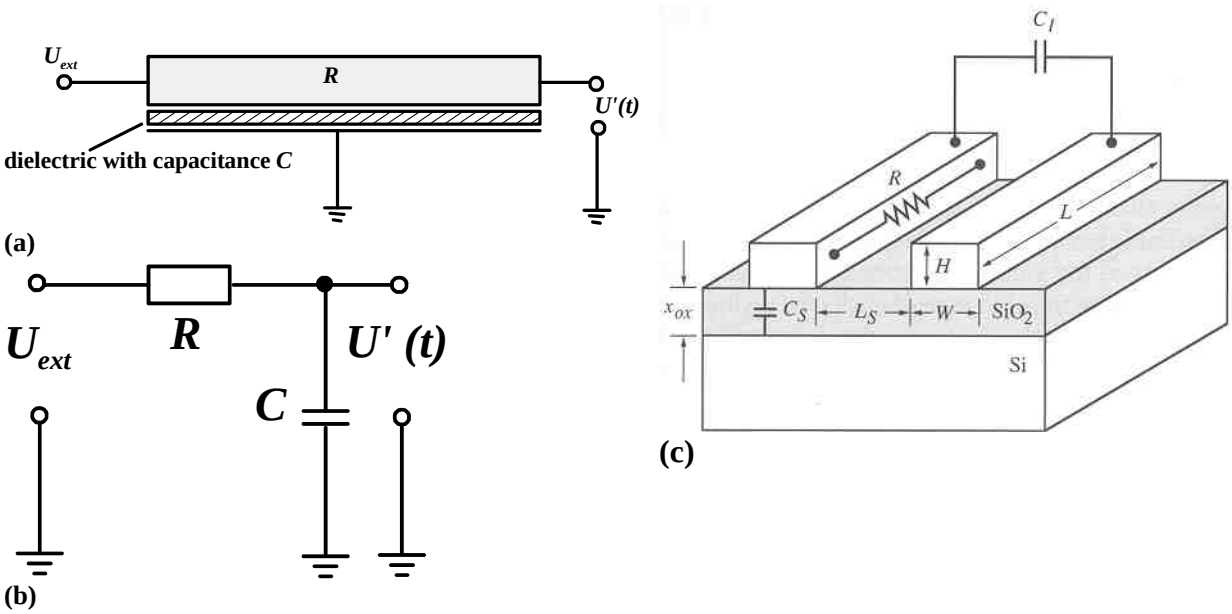

Fig. 1: (a) Basic approach to wiring delays: U_{ext} is the signal which is imposed on the wire to switch a transistor on the other end of the line. The wires have a resistance R and are surrounded by a dielectric leading to a capacity C. $U'(t)$ is the voltage which is available at a consumer, e.g. a transistor gate. **(b)** "Standard" RC delay equivalent circuit. **(c)** Interconnect lines and resulting capacitances and resistances: C_S = capacitance wire/substrate, C_I = capacitance wire/wire.

RC-delay: **Fig. 1a** sketches the cross section of an interconnect wire separated from a grounded substrate by a dielectric.

a) Describe qualitatively the transient of U' when the U_{ext} changes from 0 V to 1.5 V.
b) Describe the transient of U' when U_{ext} is switched off again.
c) Why is the delay $\tau = 0.89\ RC$ in **Fig. 1a** not completely equivalent to the delay of the circuit in **b)** ($\tau = RC$)?
d) Derive the resistance R for one of the wires (resistivity ρ) shown in **Fig. 1c**.
e) Derive the total capacitance C for one wire.
f) Give a total formula for the delay (also keep the 0.89 from **c)** in mind!).

In 1997, the SIA roadmap gives the following values for interconnects: ρ = 3.3 μΩcm, ε_{diel} = 3.5. For the following calculations: Min. feature size = $F_{min} = L_S = W = H = x_{ox}$ = 250 nm. The (maximum) length for a global interconnect is approximated by $L = L_{max} = \sqrt{A}$ for a chip size A = 300 mm^2.

g) Update your τ formula from **f)** and calculate the delay τ. Is this critical for a chip with f = 200 MHz? Why was it nevertheless possible to have 200 MHz chips?
h) What has most likely been used as metal and as dielectric?

In 2005, the ITRS roadmap gives $F_{min} = L_S = W = H = x_{ox}$ = 80 nm, and the length of a local interconnect spans max. 40 transistors, i.e. L_{max}= 40 * 2 * 80 nm = 6.4 µm.

i) Calculate τ_{new} for a local interconnect and the switching period duration for an f_{new} = 4 GHz chip. Are there critical problems arising yet?

To make interconnects faster, the new metal of choice is copper (ρ_{Cu} = 2.2 µΩcm) combined with a low-k dielectric with $\varepsilon_{ox.}$ = 2.8.

j) What is benefit for τ? How many ITRS – generations (every 2 "generations" mean a ½ τ) did the change to the copper/low-k system bring?