A Preview of The 21st Century Semiconductor Technology Short Course

A totally new Semiconductor Technology Short Course and Handbook has been developed to maximize your productivity by:

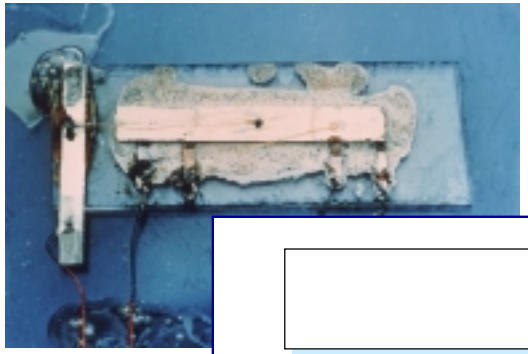
> ***making it easier to develop a much better understanding of how devices work and how they are built and how all the pieces fit together***
>
> ***providing you with the most complete, up-to-date, real-world information you need to meet the challenges facing today's rapidly changing semiconductor industry***

Picking the right course is important. To help you appreciate our course, the following pages provide an extended overview of the material typically presented. All of this material is in the Handbook. We invite comparison with any other course.

Course participants also receive our 600+ page Semiconductor Technology Handbook and the companion CDROM which provides a full-color copy of the Handbook and all of the slides presented in the course. The Handbook/CDROM is also sold separately.

For information on upcoming courses contact SemiTracks at www.semitracks.com.

The First Integrated Circuit



Jack Kilby, Te

Note that external wires are

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Industry Experts Are Raising Serious Concerns About The Next Decade

"No known solutions…the most difficult challenge the semiconductor industry has ever faced."

"In the next 5-10 years, we expect more chip manu-facturing changes than in the vious forty years."

What's Up From SEMI

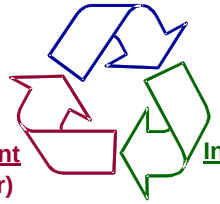
e experts predict] will hit a vall in the next 10 years ng Moore's Law and rocking miconductor industry from ndations."

Tom Murphy, Electronic News

Introduction-16

Moore's Law Cycle

Every 2– 3 Years:
- Double Performance
- Double Transistors/Chip (Original Moore's Law)
- Halve Cost/Transistor



Growing Investment
- Fab (+25%/year)
- R&D

Increasing
- Sales (+15%/year)
- Profits

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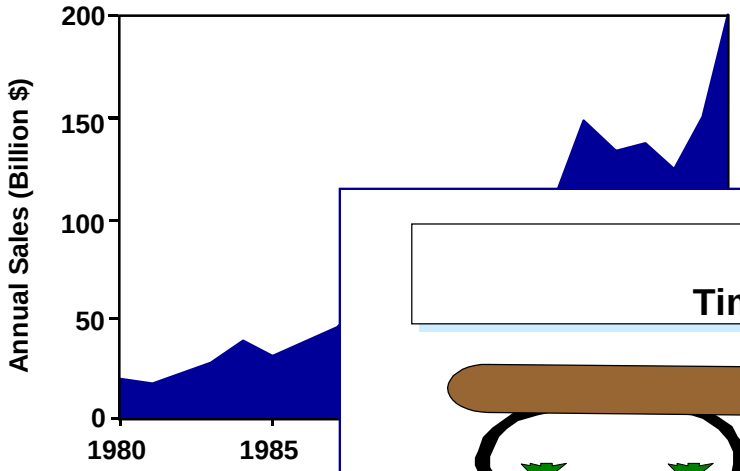
Introduction-14

***INTRODUCTION*: You will learn the history of Integrated Circuits, the "Moore's Law Cycle" that drives the industry forward and the future challenges facing the industry.**

Annual Semiconductor Sales:
Periods of (mostly) Boom and (some) Bust



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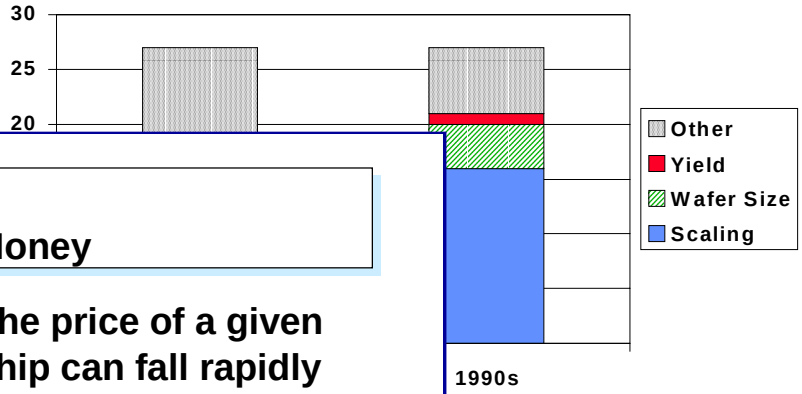
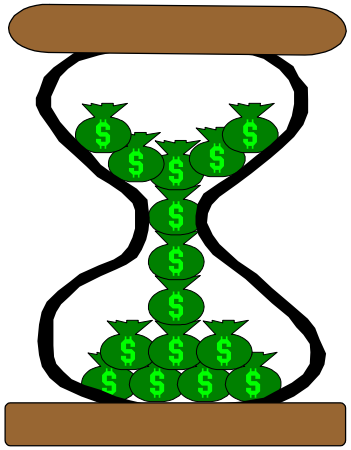
The Changing Mix of Improvements That Results in Lowered Cost/Transistor



Economics 18

Time Is Money



- The price of a given chip can fall rapidly with time
- The cost/hour of running a fab is increasing
- Have to halve the cost per transistor every 2-3 years

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Economics 8

***ECONOMICS*: You will learn about the all important economic factors that shape the direction of the semiconductor industry.**

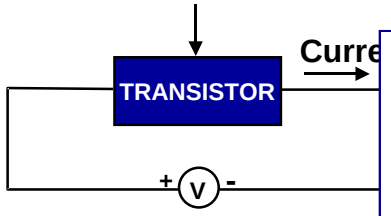
Two Types of Transistors: Voltage Controlled & Current Controlled

Field Effect (MOS) Transistor

Bipolar Transistor

Gate Voltage

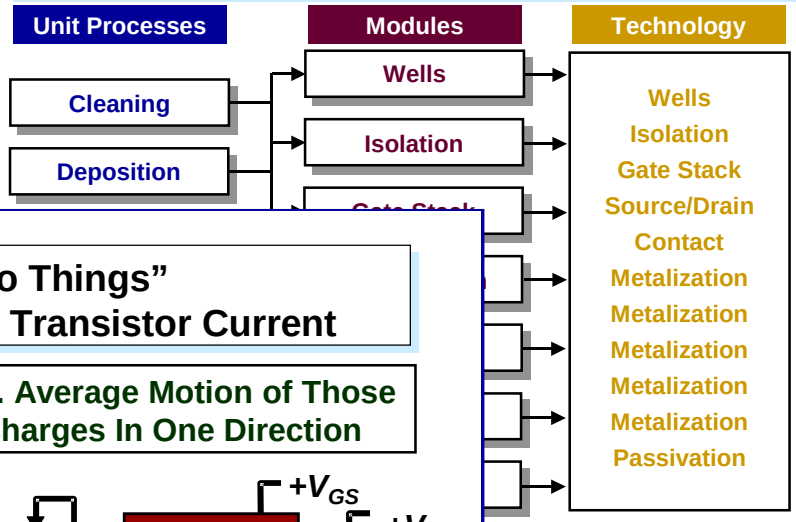
Base Current



MOS are the most widely used be

Bipolar transistors are used in ni

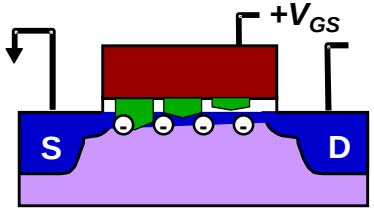
Overview of Processing: *Unit Processes to Process Modules to Technology*

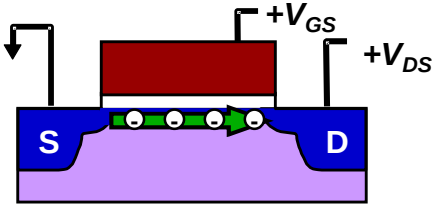


"Only Two Things" Are Required For a Transistor Current

1. Mobile Charges

2. Average Motion of Those Charges In One Direction

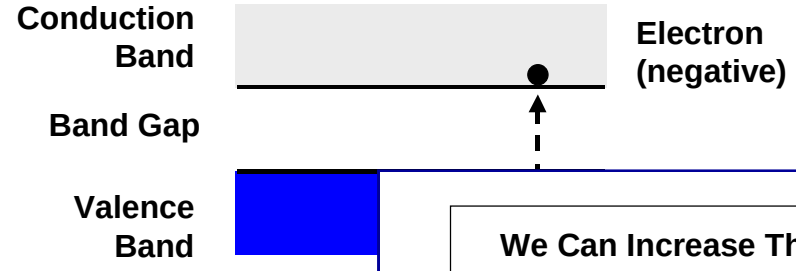




- A <u>Gate Voltage,</u> $V_G > V_{THRESHOLD}$ creates a surface layer of mobile charges ("inversion")
- <u>Drain Voltage</u> produces an electric field which moves electrons from source to drain

***<u>TECHNOLOGY OVERVIEW</u>** You will get a review of background material and then receive an overview of how transistors work and how they are built. This section will help you to put the detailed material that follows into perspective.*

Electrons and Holes



- Electrons in conduction b
- The vacancy created by a band can be considered a which moves in the *valan*
  - use the symbol e^+ or p^+ t

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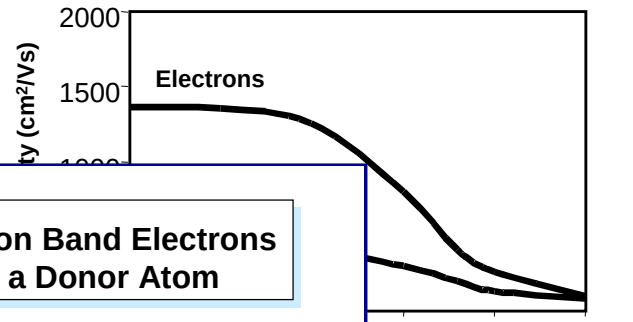
Electron Mobility Is Higher Than Hole Mobility

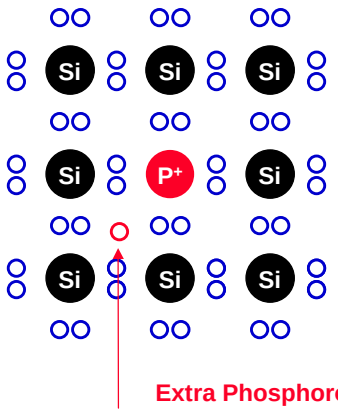


evel (cm^{-3})

hannels is lower

Semiconductors 30

We Can Increase The Conduction Band Electrons By Doping The Lattice With a Donor Atom



- Phosphorous has 5 valance electrons
- Only 4 are needed for covalent bonding
- The 5th. electron is very loosely bound and can easily go into the conduction band
- This leaves behind a positively charged phosphorous ion
- Phosphorous is called a "donor" material
- Resulting material is n type (because of excess electrons)

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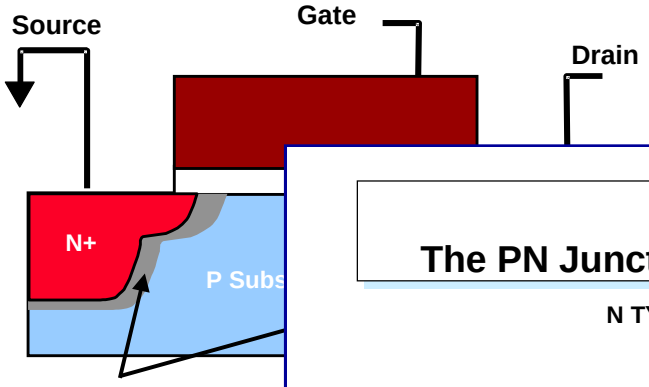
Semiconductors 14

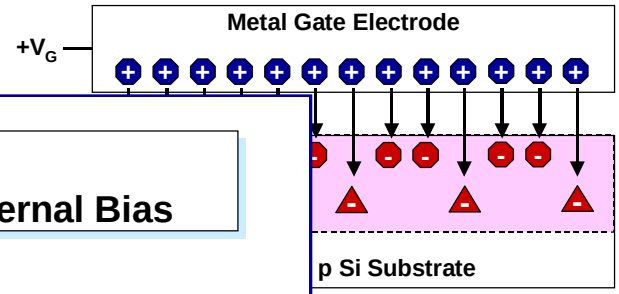
SEMICONDUCTOR BASICS *You will learn the basic of semiconductors including bands, electrons and holes, how to change electron and hole concentrations by doping and how to produce currents in semiconductors (drift and diffusion).*

The MOS Transistor Consists of a MOS Capacitor and Two Diodes



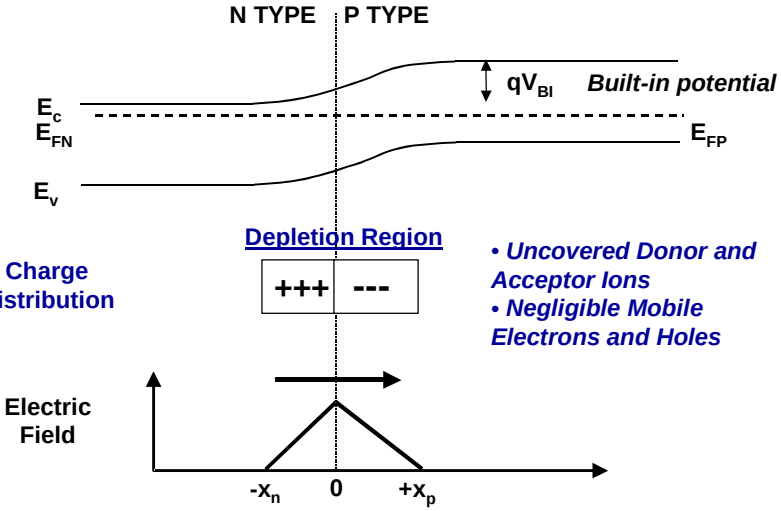
Diodes

MOS Capacitor: Gate and Silicon Charges



e amount of positive charge on
he inversion layer
ions in depletion layer

The PN Junction With No External Bias

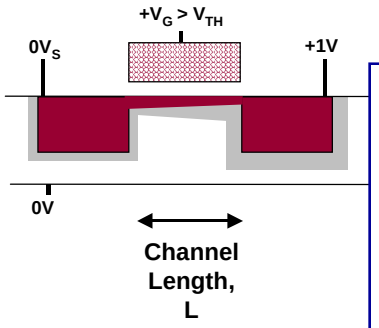


- *Uncovered Donor and Acceptor Ions*
- *Negligible Mobile Electrons and Holes*

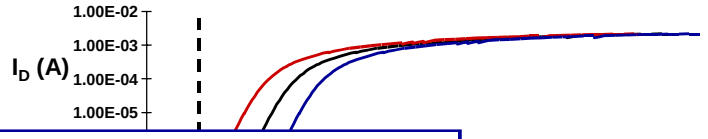
DIODES AND MOS CAPACITORS *You will understand what happens when a pn junction is formed and the effects of external biases on depletion regions and currents. You will know the basic operation of the MOS capacitor, how inversion layers form and the factors that influence threshold voltage.*

Estimating Currents: *Low V_D - Linear Region*

- Above threshold, behaves like a simple capacitor
  - $Q_{CH} \sim C_{OX} (V_G - V_{TH})$
- Average field across the channel



Small Changes In Threshold Make Very Large Changes In Leakage Currents



V, $I_D(V_D=0)$=**10,000pA** (Calculated)

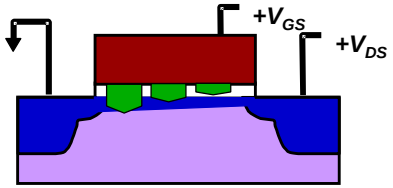
V, $I_D(V_D=0)$ = **100pA**

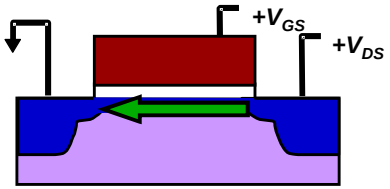
V, $I_D(V_D=0)$ = **1pA** (Calculated)

.5 2.1 2.7

Ideal Transistors 27

V_G Produces The Mobile Carriers and V_D Makes Them Move From Source to Drain





- **Gate Voltage Produced Vertical Electric Field**
- **$V_G > V_{TH}$ creates a surface inversion layer of mobile charges**
- **Drain Voltage Produced Horizontal Electric Field**
- **Goes from drain to source**
- **Causes drain current**

Ideal Transistors 6

IDEAL TRANSISTOR *Our unique "Only Two Things" approach will let you understand how transistors really work. You will understand the linear, saturation and subthreshold leakage modes of transistor operation.*

Two Scaling Scenarios: High Performance and Low Power

- **Optimizing for high performance**
  - higher V_{dd}
  - and/or lower V_{th}
- Performance increases because saturation curre increases ~ $(V_{dd}-V_{th})^n$
  - higher "gate overdrive"
- However
  - higher V_{dd} - higher active a standby power
  - lower V_{th} – higher standby power
- **Optimizing for low pow**
  - lower V_{dd}
  - and/or higher V_{th}
- Less performance

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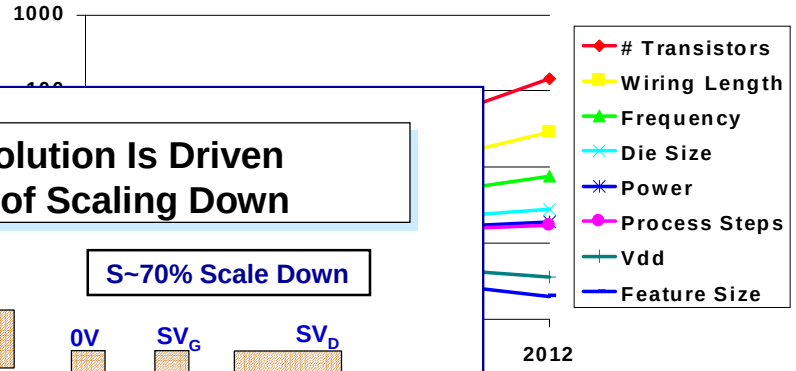
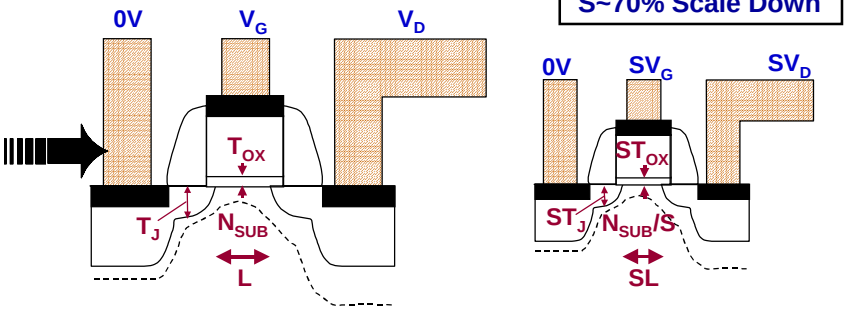
Relative Scaling of Key Integrated Circuit Attributes



Source: 1997 NTRS

Scaling 10

The Silicon Revolution Is Driven By The Benefits of Scaling Down



Speed*	*Increases by 40%*
Transistors/Chip*	*Double*
Power/Chip*	*Constant*
Insulator Reliability*	*Constant*

** Ideal Constant Field Scaling with fixed chip area*

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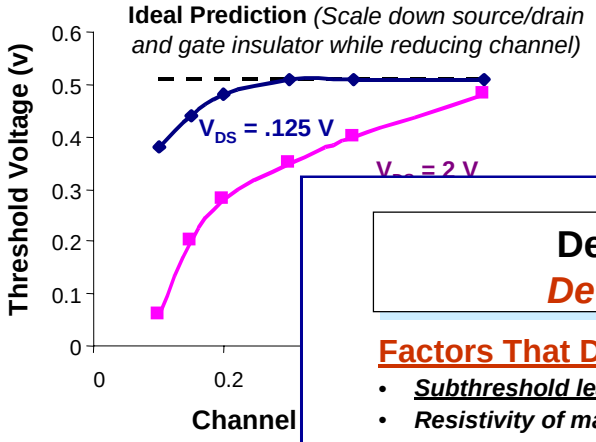
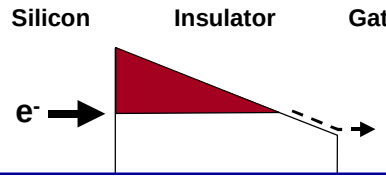
Scaling 6

SCALING *You'll understand how transistors get better with scaling and the different scaling approaches used for optimizing performance and for low power.*

The "Short Channel" Effect Causes Threshold Voltages to Fall



Very Large Direct Tunneling Currents Are Possible When Gate Insulator Is Too Thin



- Large barrier for electron tunneling
- Finite, but very small, silicon-to-gate current
  - Called Fowler Nordheim injection

- Thinner oxide
- Smaller barrier
- Tunnel directly from silicon to gate
- Much larger currents
  - Currents grow exponentially larger as barrier is reduced

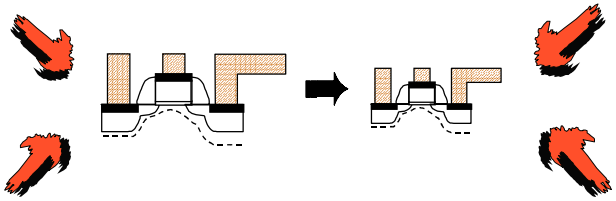
Deep Submicron Scaling: *Device Physics Challenges*

Factors That Do Not Scale

- ***Subthreshold leakage***
- ***Resistivity of materials***
- ***Cross talk***

Short Channel Effects

- ***Threshold rolloff***
- ***Increased leakage***
- ***Punchthrough***



High Field Effects

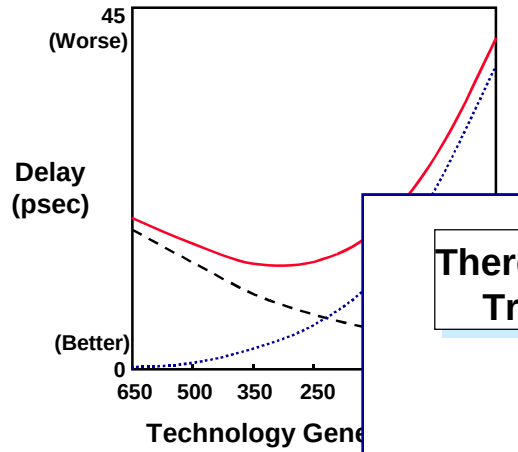
- ***Velocity saturation***
- ***Gate induced drain leakage***
- ***Reliability***

Thin Gate Effects

- ***Tunneling***
- ***Poly depletion***
- ***B penetration***

NONIDEAL EFFECTS ***You'll have an introduction, in easy-to-understand terms, of the non-ideal effects in transistors including the short channel effect, tunneling through the gate insulator and velocity saturation.***

Interconnect Is Becoming Increasingly Important in Determining Delay Time



Transistor alone

Al/SiO2 interconnect alone

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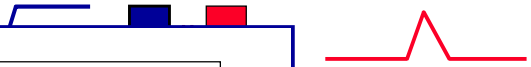
Crosstalk Between Adjacent Interconnect Lines Is a Growing Concern

A Normal Pulse on the "Aggressor" Line

Can Induce a Parasitic Pulse on "Victim" Line



C_V)

width) of lines

pacting density

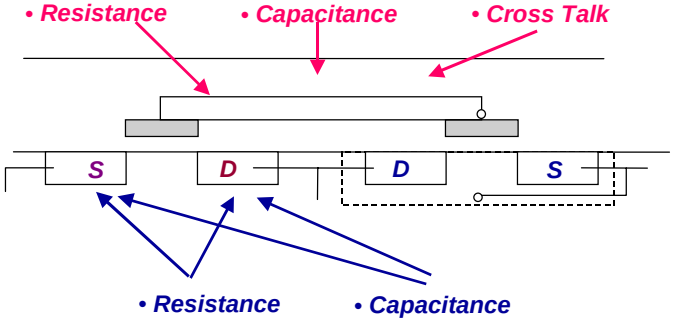
vertical capacitance

Parasitics13

There Are Parasitic Elements Associated With Transistors and Interconnections (Metal)

Interconnect Parasitics

• *Resistance* • *Capacitance* • *Cross Talk*



• *Resistance* • *Capacitance*

Transistor Parasitics

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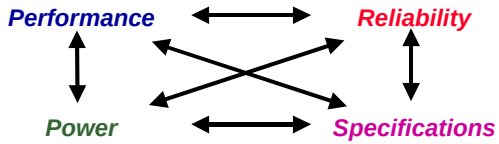
Parasitics3

PARASITICS *You'll understand the growing problems with parasitic resistances and capactitances and how to manage them.*

Performance, Power, Reliability and Specifications Are Being Traded Off



"[Power, performanc
optimized simultane

so there needs to be
three constraints"

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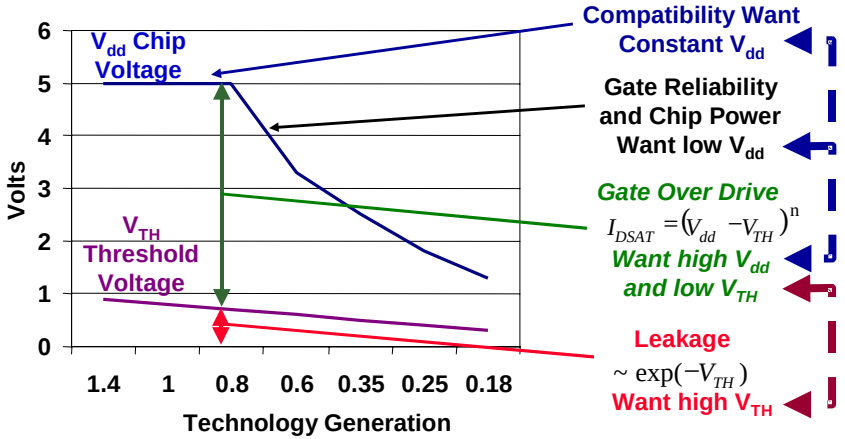
Selecting Chip (V_{dd}) and Threshold (V_{th}) Voltages for Performance Or Low Power

1980s 1990s 2000s

High Performance
-Higher V_{dd}

We Are Faced With Tradeoffs When Choosing Chip and Threshold Voltage



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Tradeoffs 10

Tradeoffs 12

TRADEOFFS *You'll understand that tradeoffs are required to develop technologies focusing on the all-important power versus performance tradeoff.*

What Do We Want From: *The Starting Silicon Wafer?*

- **Single crystal of Silicon**
  - *Electrical properties depend on crystalline nature*
- **Thin top region (**
  build the transi
  - *Free of defects tha*
  - *Low level of intenti*
  precisely tailor the
- **Thick bulk of the**
  - *High level of intent*
  inhibits unwanted
  - *Ability to trap defe*
  active region ("inte

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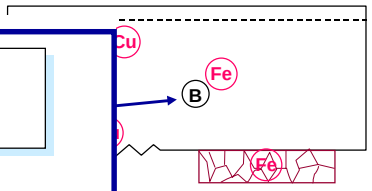
Intrinsic and Extrinsic Gettering

INTRINSIC GETTERING

Impurity decorating oxygen

Front side Active Region



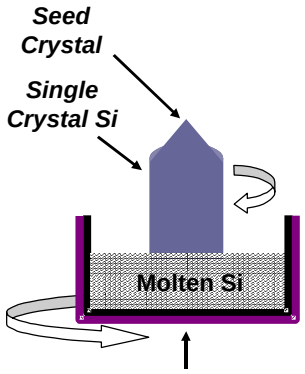
ide
nical
ge

Backside Polysilicon

TRINSIC GETTERING

Starting Materials 28

Czochralski (CZ) Crystal Growing



- **Start with molten silicon in a SiO_2 crucible**
  - **Add desired impurities to the melt**
- **Withdraw a rotating seed crystal**
  - **More rapidly at first to form thin neck region that traps imperfections**
  - **Followed by a slower pull which produces a larger diameter wafer**

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Starting Materials 14

STARTING MATERIAL. ***You'll learn how silicon wafers are manufactured.***

Importance of Cleans

- Particles and contaminants
  - Can "kill" an integrated circuit
    - Newer technologies are sensitive to smaller
  - Are present i
  - Are generate
  - Are generate
- Cleans are u
  - Different type
    - e.g., clea
- Also critical
  - Laminar flow
  - Ultrapure wa
  - Equipment d
  - Eliminate hu

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Common Cleans

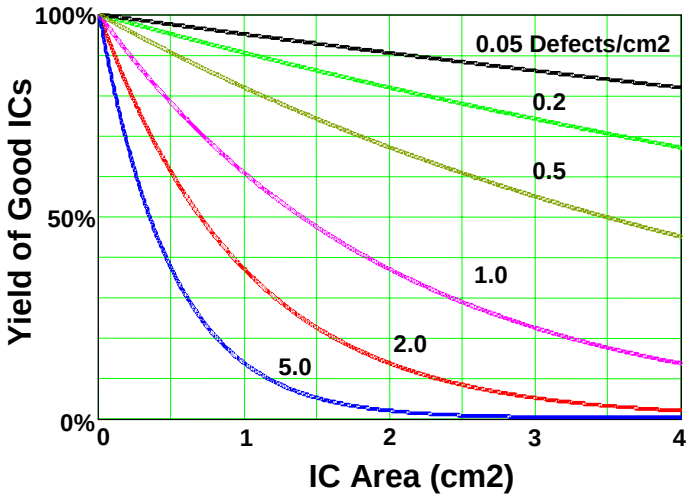
- Front End of Line

aggressive cleans
(SC1) and (SC2)
$H_20+H_2O_2+NH_4OH)$
($H_2O+HCl+H_2O_2$)
$_4$)

ggressive acids and

Cleaning 13

Yield Decreases Rapidly As the Defect Density Increases



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Cleaning 4

CLEANING *You'll learn about the processes used to clean wafers.*

Photo Lithography Process Flow

Dehydration	*Remove moisture for PR adhesion*
Prime	*Coat (e.g., HMDS) to further improve adh*
Spin-On PR	*Depo*
Bake	*Drive*
Expose	*Trans*
Develop	*Remo*
Etch or Implant	*Trans*
Strip PR	*Remo*

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Techniques for Enhancing Lithography: Mitigating The Effects of Diffraction

Optical Proximity Correction

Ordinary

- Wavefront Engineering
  - Enhance the high spatial frequency component of the illumination
  - Phase Shifting
  - Off-axis illumination

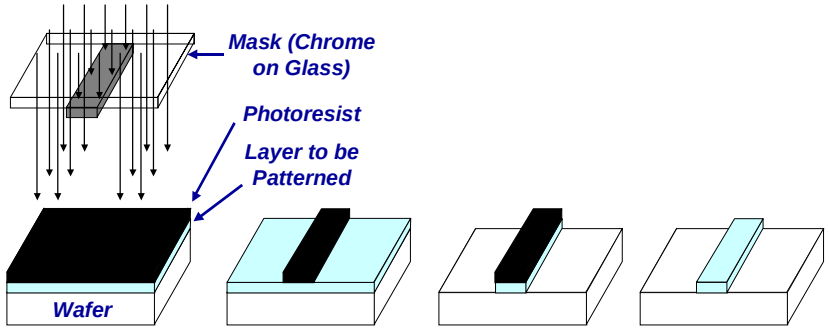
ptical Proximity
orrection (OPC)
- modify mask to compensate for distortion in processed image

esult: can print features
t or slightly below the
ave length of the light
- minimum channel lengths approaching 1/2 litho wavelength

Lithography 45

Pattern Definition Using Positive Photoresist

1. Coat With Photoresist
2. Expose Through Mask
3. Develop (Dissolve Exposed Resist)
4. Use Resist As An Etch Mask *(Alternative: Use as Implant Mask)*
5. Strip Photoresist



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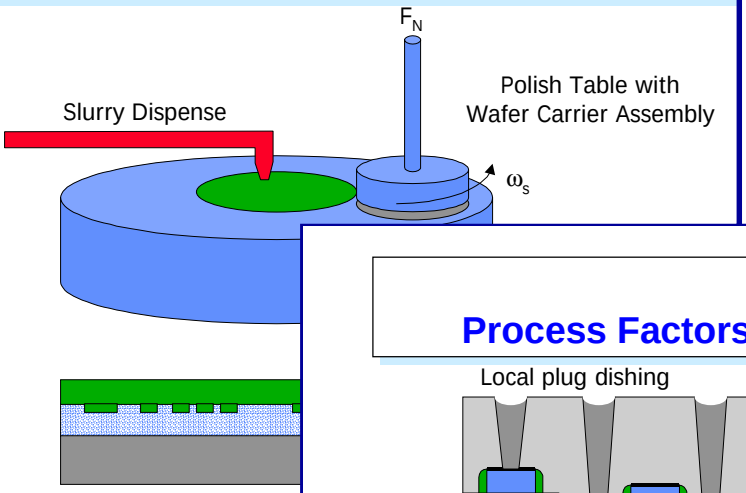
Lithography 26

LIITHOGRAPHY. *You'll learn the basics of lithography including advanced techniques for extending resolution.*

Diagram of CMP Process



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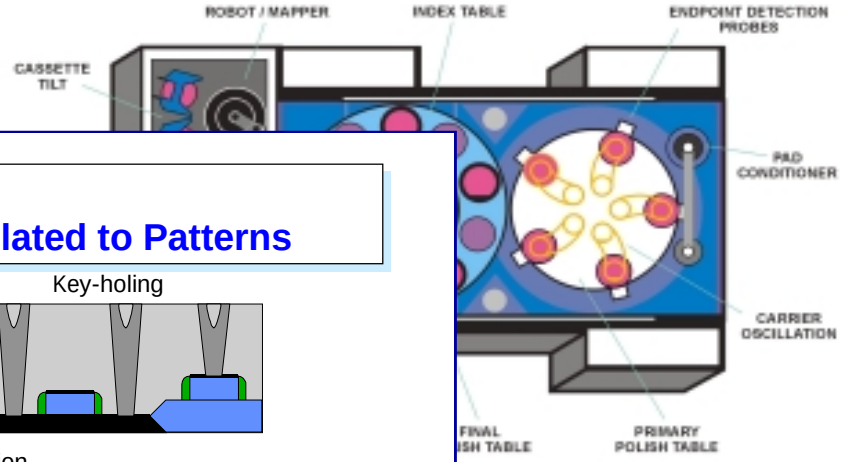
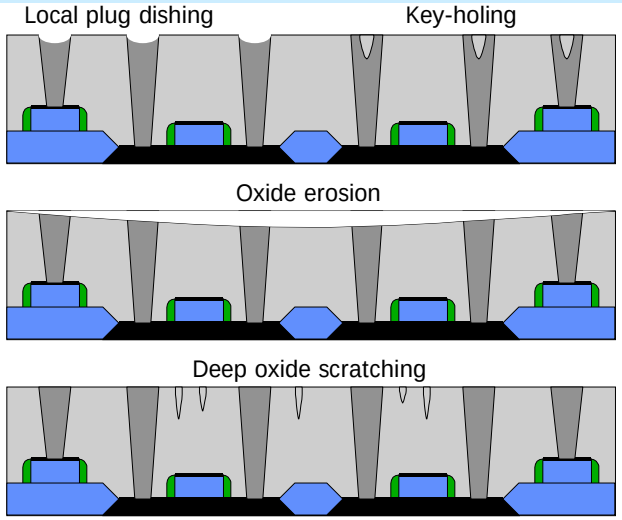
Internal Tool Layout Example



eedfam-IPEC

Process Factors Related to Patterns



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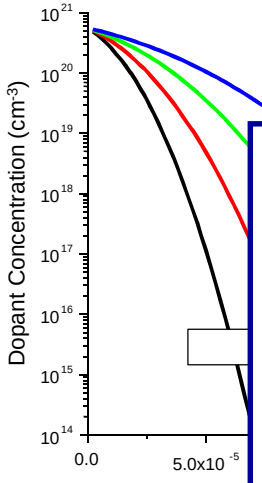
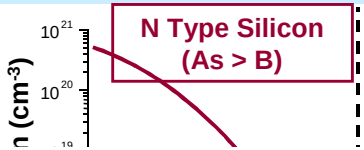
PLANARIZATION. ***You'll learn about the processes used to planarize wafers, especially Chemical Mechanical Polishing (CMP).***

Diffusion from an Infi
(E.g., Doping From Exte



- Examp
  - D =
  - N_0 =

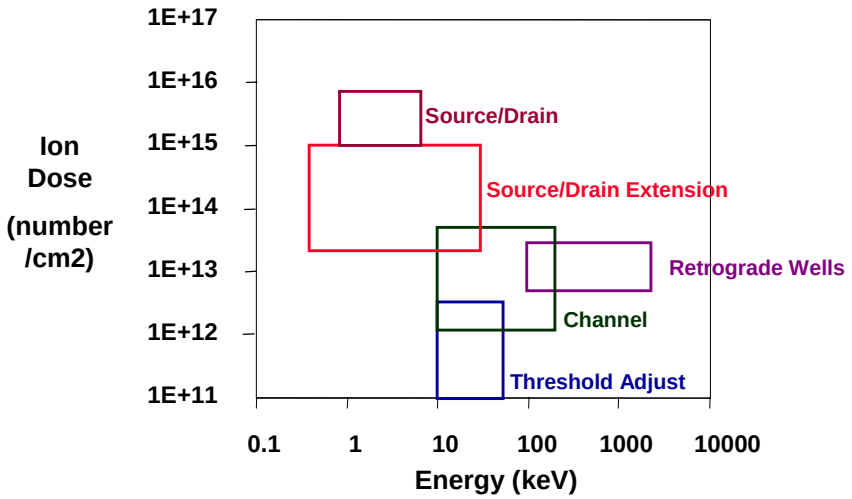
Junction Depth Example:
As Surface Diffusion Into B Doped Wafer



ground
oping

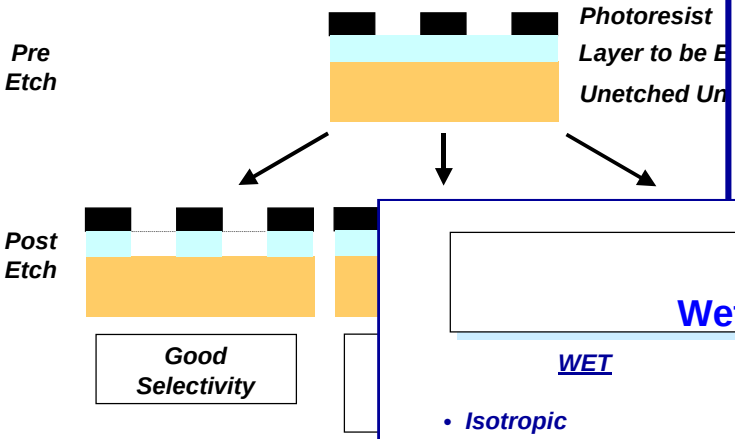
2.5x10 -4
m)

Representative Doses and Energies
Used to Form Key IC Features



<u>DIFFUSION AND IMPLANTATION.</u> ***You'll learn the processes that are used to introduce dopants into the silicon wafer.***

Etch Selectivity: *Etch What You Want Don't Etch What You Don't Want To*



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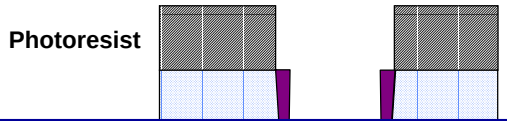
Etching High Aspect Ratio Features Using Sidewall Polymer Formation



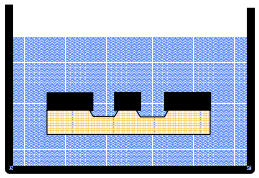
- The chemistry of the etchant is adjusted such a polymer will form on the sidewalls
- Polymer prevents sidewall etching leading to highly anisotropic etching

Etching 9

Wet and Dry Etching

WET

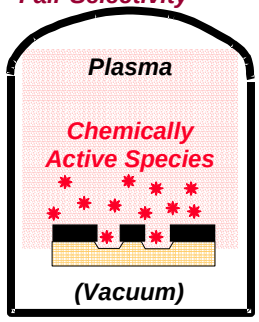
- *Isotropic*
- *Good Selectivity*
- *Environmental Issues*



DRY

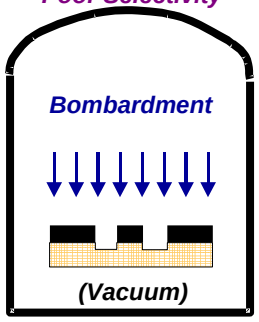
1. PLASMA ETCH

- *Isotropic*
- *Fair Selectivity*



2. SPUTTERING

- *Anisotropic*
- *Poor Selectivity*



3. REACTIVE ION ETCHING
- Controlled Anisotropy - Better Selectivity

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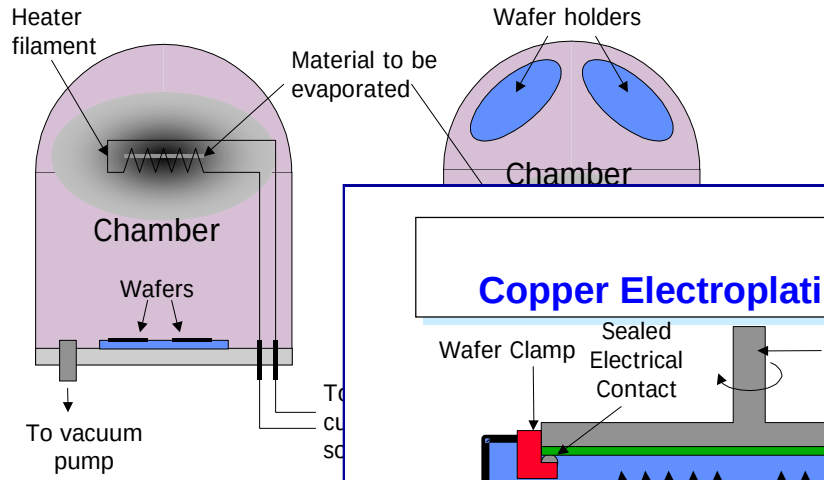
ETHCING. *You'll become aware of wet and dry etching and the damascene process.*

Filament and Electron Beam Evaporation



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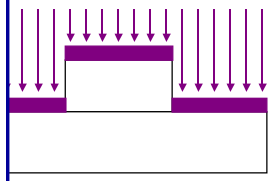
onformal (CVD) vs. Nonconformal (PVD) Deposition

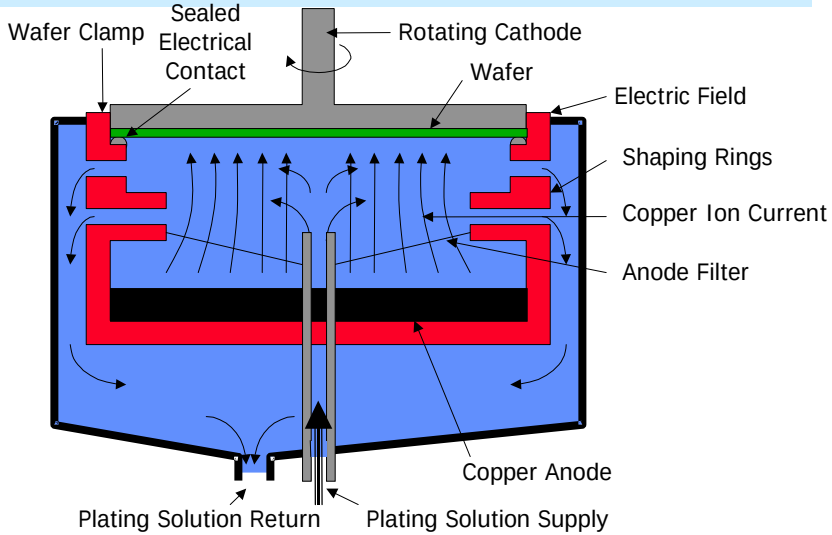
CVD
Conformal Coating

PVD
Nonconformal Coating



Semiconductors 27

Copper Electroplating System Diagram



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FILM DEPOSITION. ***You'll know the main ways of depositing thin films including CVD, PVD and electroplating.***

Attributes Of The Different Ways To Deposit Thin Films

Method	Type	Consume Si?	Conformal Coating?	Temperature
Reaction with Si Wafer	Chemical Reaction	Yes	Yes	High
Physical Vapor Deposition (PVD)	Physical Deposition	No	No	Low
Chemical Vapor Deposition (CVD)	Chemical Reaction			
Plasma CVD (PECVD)				
Electroplating From Solution	Chemical Reaction			
Spin-on Films	Physical Deposition			

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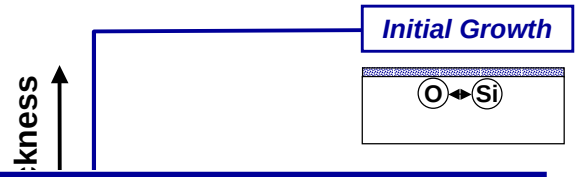
Deal-Grove Oxidation Model

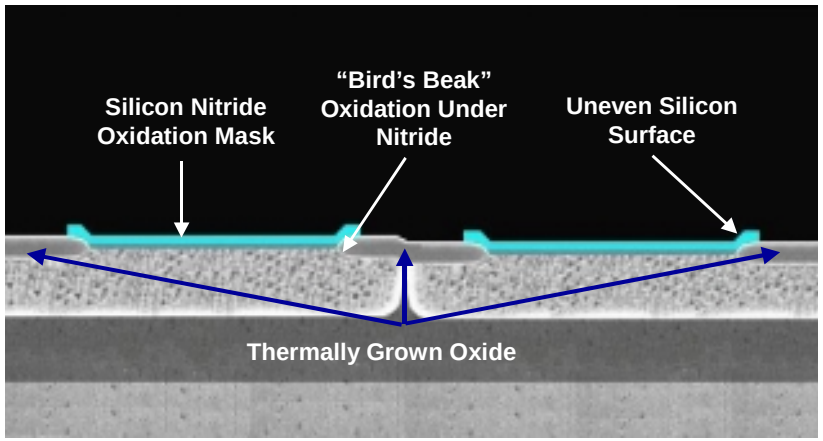


- Easy for O to diffuse through thin oxide
- Oxidation limited by reaction with Si
- Linear growth

- Oxidation limited by diffusion through thicker oxide
- Parabolic growth

Oxidation 8

Oxide Forms Under Edges of Nitride Mask ("Bird's Beak")



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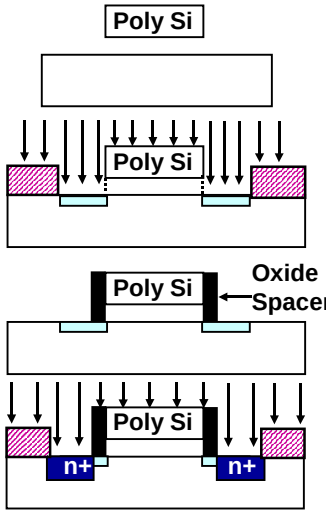
Oxidation 20

OXIDATION. *You'll learn about thermal oxidation of silicon.*

History of The Source and Drain: 4. Shallow Source/Drain Extension



- In the 1990s
  - *Less of a concern for hot carri*
  - *degradation as supply voltage*
  - *decrease*
- S
- Ic

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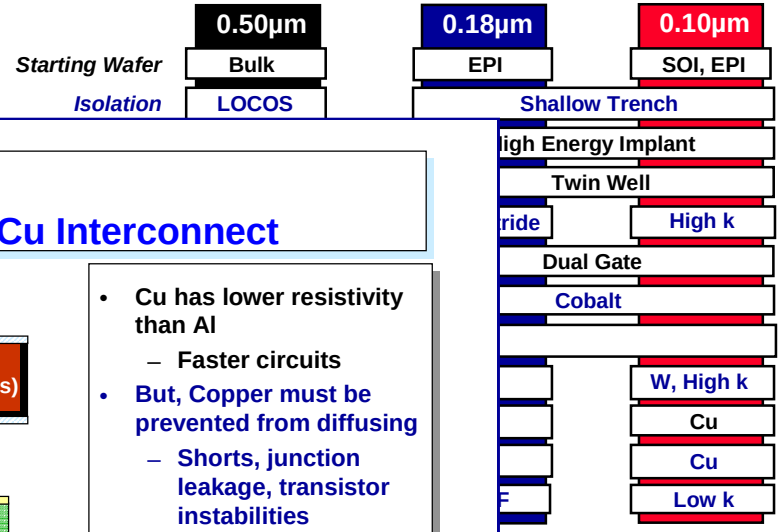
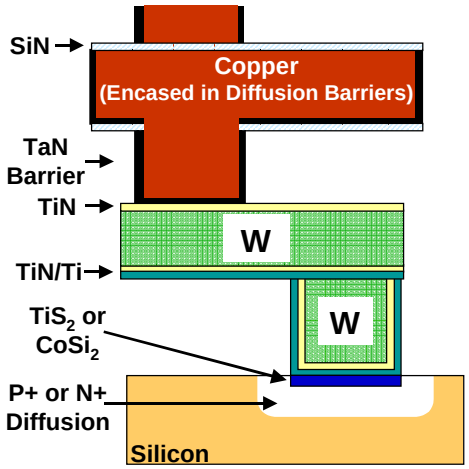
Evolution of CMOS Technology: 0.50µm to 0.18µm (1999) to 0.10µm (2005)



Process Integration 57

Schematic of Cu Interconnect



- Cu has lower resistivity than Al
  - Faster circuits
- But, Copper must be prevented from diffusing
  - Shorts, junction leakage, transistor instabilities
  - Line bottoms and sides with barrier metal
  - Use nitride cap
  - Use W, not Cu, for first level interconnect

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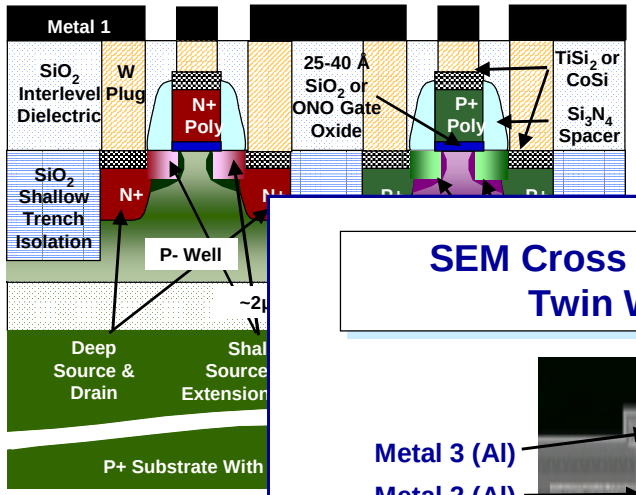
Process Integration 52

<u>PROCESS INTEGRATION</u> *You'll learn how the unit processes are integrated into the Front End of Line (Isolation, Wells, Gate Stack & Source/Drain) and Back End of Line (Contact, Metalization, Passivation) process modules. For each module you'll know how the modules changed over time and what are the pros and cons of the various alternatives.*

Representative 0.18 Micron Transistor Technology



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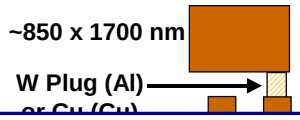
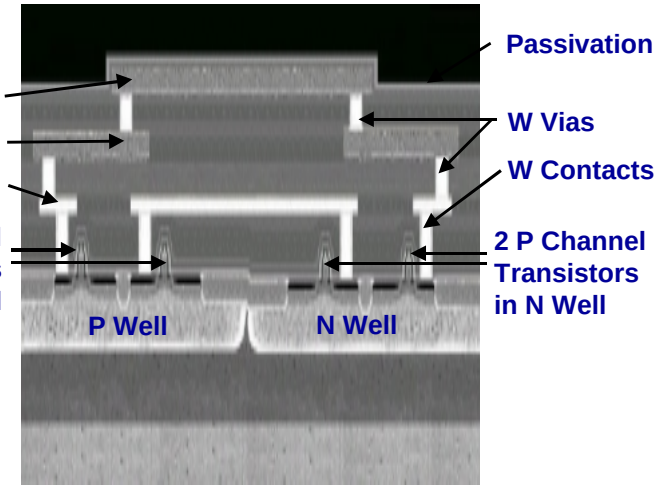
0.18 Micron Technology Interconnect



- ~6 layers of interconnect
- Aspect ratio (H/W) ~ 2
  - high density, lower resistivity
- ower layers are local terconnect
- pper layers are global terconnect
  - thicker and wider
- nes are Al or Cu with /TiN barrier layers
- plugs
- ower K interlevel electric to reduce C
  - reduce speed & crosstalk

0.18µm Technology-33

SEM Cross Section of 3 Level Metal, Twin Well, 0.18µm CMOS



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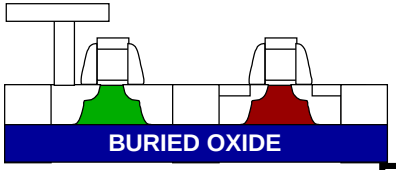
0.18µm Technology-34

<u>STATE OF THE ART 0.18 MICRON TECHNOLOGY.</u> You'll learn about a complete, state-of-the-art 0.18 micron technology flow from step-by-step diagrams and from actual scanning electon microscope pictures. .

Silicon on Insulator



- Starting to see increased use of SO
- **Advantages**
  - reduces source/drain capacitance (speed)

- ***IBM reported a 150nm buried oxide for their high performance 0.18µm technology*** *(Leobandung et. Al., 99 IEDM)*

From late 90's to late 00's We Could Change Almost All of The IC Materials

Circa late 1990s

Circa late 2000s

- Metal(s) (TBD)
- High K (TBD)
- Cu (followed by optical?)
- Low K (organic, aerogel)
- SiGe
- Silicon on Insulator
- High K (ferroelectric?)

historic exponential quivalent Scaling"

Advanced Technology Options: *Potential Benefits*

Technology Change	Per-form-ance	Power	Reli-ability	Parasitic Resistance		Parasitic Capacitance	
				Tran-sistor	Inter-connect	Tran-sistor	Inter-connect
Cu	■		■		■		
Low K interlevel	■						■
High K gate diel.		■	□				
Metal gate	■	□		■ (G)			
Raised S/D	■			■ (SD)			
Si/Ge Channel	■						
SOI	■	■	■ (SEU)			■	
Dual Gate		■					
Low Temperature	■	■	■				
Dual Threshold	■	■					
Optical Interconnect	■				■		■

FUTURE TECHNOLOGY CHALLENGES *You'll learn about the potential solutions to meet the challenges facing current and future generations of technology.*

Now A Third Scaling Scenario Is Emerging:

Optimized for Integration of Multiple Technologie

1980s 1990s 2000s

High Performance

Pow

Many companies are looking fo
technology limits and without r

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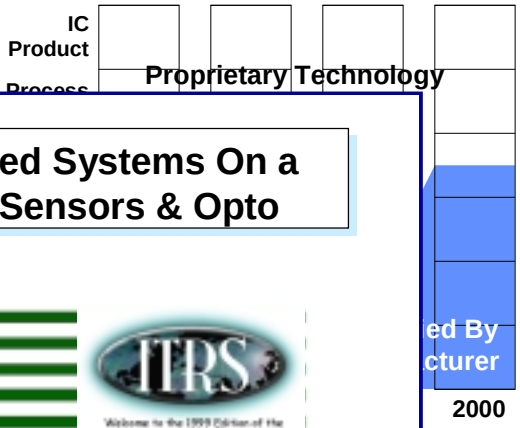
The Role of Equipment Suppliers Is Expanding



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ost, Applied Materials, 1998 IRW

Industry Trends 10

The 1999 Roadmap Added Systems On a Chip Including MEMS, Sensors & Opto

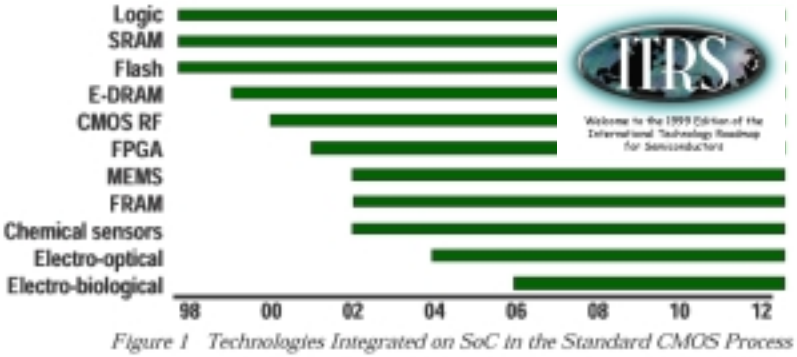

Figure 1 Technologies Integrated on SoC in the Standard CMOS Process

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Industry Trends 13

INDUSTRY RESPONE TO CHALLENGES ***You'll learn how the industry is changing to meet the future economic and technical challenges.***