PAPER REFERENCE: E-III.1

New Developments in Silicon Czochralski Crystal Growth and Wafer Technology

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Abstract:

An overview of recent progress in large diameter crystal pulling and associated new wafer preparation technologies is given. A clear trend can be observed that with increasing crystal diameter, the average oxygen concentration and the density of intrinsic grown in defects is requested to be reduced. Oxygen reduction and control is achieved by using magnetic fields, while bulk defect reduction requires sophisticated hot zone engineering. New growing methods currently under development result in new crystal types with a high density of interstitials in the outer area and lower density of vacancies in the center. In addition, crystals are grown under near equilibrium conditions so the super-saturation of the intrinsic point defects remains below the critical value required for clustering of the point defects into larger agglomerates . Geometry and LPD/LLS requirements for future wafer generations are becoming more stringent with each decrease in design rule. This leads to the necessity of novel wafer surface preparation methodologies such as advanced single side polishing (SSP), double side polishing (DSP) and plasma assisted chemical etching (PACE) with local wafer surface treatment. Finally, the trend toward low thermal budget integrated circuit processes leads to the necessity of having oxygen precipitation tuning (PT) and GOI tuning (GT), as well as the creation of a denuded zone by the silicon wafer manufacturer. New approaches to meet these requirements are annealing at high temperature and/or rapid thermal processing. The development of the new epitaxial wafer types is highlighted.

Keywords:

Microelectronics, Technology Roadmap, Silicon Wafer Technology, CZ growing,

1. Introduction

The technological engines in microelectronics are the developments in memory devices and microprocessors. The DRAM memory devices determine the smallest structure size and the highest device complexity, while the microprocessors set the benchmark for the clock frequency speed. At the end of the millenium (1999) worldwide introduction of 256 Mbit DRAMs in 0.18 μm technology as well as Intel's Pentium III microprocessors with a 500 MHz clock frequency is at the introduction stage to the market place. Predictions for the year 2009/2012 include DRAM memory devices in 35 nm technology with a capacity of 64 Gbit and microprocessors with a clock frequency of 10 GHz in silicon technology.

The development of Silicon Technology, which has to support each of these advanced applications, is consequently reflected in the Technology Roadmap. The Semiconductor Industry Association (SIA) National Technology Roadmap for Semiconductors (NTRS) [1], now known as the International Technology Roadmap for Semiconductors (ITRS) was first published in 1994 and revised four times in the meantime.

Year	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012
94 NTRS Roadmap			180			130			100					
97 NTRS Roadmap	180		150		130			100			70			
98 NTRS Roadmap	180			130			100			70				35
99 ITRS Proposal	180		130		100		70		50		35		25	

Table 1: SIA-ITRS Roadmap; Minimum feature Size in Nanometers

A comparison of the different ITRS Roadmap versions shows that in a time period of five years (from 1994 to 1999) introduction of smaller design rules has shortened from an original three year interval to a two year interval with a tendency to accelerate even more. Until now three years had passed between the introduction of subsequent design rule generations, and currently a design rule life cycle of two years is being predicted. If this trend in the design rule shrink continues, Moore's Law will even be surpassed [2]. A slow down due to technological reasons is not seen presently. Furthermore, the increase in wafer size in the ITRS Roadmap has to be emphasized. At the moment (1999) 200 mm wafer diameter is state of the art. The diameter will increase to 300 mm (introduction into mass production in 2001), later on to 450 mm (introduction into mass production in 2009) and eventually the 675 mm wafer diameter is anticipated in 2015.

As the semiconductor industry moves towards larger wafers with smaller design rules, the key challenges facing silicon wafer manufacturers during the next decade are:

CZ crystal growth

1. Increased silicon crystal perfection by bulk defect reduction
2. Manage the wafer size transition from 200 mm to 300 mm

Wafering part

3. Tighter flatness requirements due to the decreasing design rules
4. Reduction in size and density of LPDs / LLSs on the wafer surface

Heat treatment and advanced epitaxy

5. Introduction of new 200 mm wafer types, such as so-called Perfect Silicon Wafer, PT Wafer, GT Wafer, HAI-wafer and smart cut/thin film SOI Wafer
6. Appearance of advanced epi products such as fLASH epi-Wafer

Changing Market

7. Changing market conditions
8. Extreme cost constraints

2. Key Challenges for the Silicon Wafer Manufacturers

2.1. Increased silicon crystal perfection by bulk defect reduction

The key areas of Czochralski (CZ) grown silicon activities is centered around four sections:

a) v/G(r) > Ccrit with the domain of vacancy related point defects
b) v/G(r) < Ccrit with the domain of interstitial related point defects
c) perfect bulk silicon which is a combination of a) and b) and "completely" free of agglomerated point defects
d) Oxygen precipitation behavior and its control

In this grouping v/G(r) is the ratio between pulling speed of the crystal and the axial temperature gradient G(r) at the silicon melt solid interface, according Voronkov`s theory [3].

Option a): In the past Czochralski silicon crystals were grown under conditions leading to material rich in vacancies. For years these crystals have resulted in wafers which show excellent yield and performance data during IC device processes and have been the material of choice for larger design rules. However, with stringent design rules these crystals reach their limitations. The crystals show a high degree of COPs (D-defects) which lead to an unacceptable high level of small LPDs/LLSs (<0,12 μm). A higher COP density degrades the gate oxide integrity (GOI) to a lower level. Combining GOI tuning via hot zone engineering with slower pulling speed results in standard vacancy rich ingots with a GOI increase of about 10-15 % to a maximum

GOI level of about 70-80 %. The limitation of this approach is the agglomerate of the COPs to sizes larger than 0.12 μm.

Option b): The main CZ activities today are focused on the regime of interstitial related intrinsic point defect control and keeping their concentration below a critical value in order to avoid the clustering of these defects. Wafers, manufactured from these ingots show much a lower LPD/ LLS densities and better GOI performance, but if the interstitial point defects are not properly controlled, these wafer do not show good device yield data in advanced low thermal budget IC device lines due to the existence of larger dislocation type defects.

Option c): Since the typical defect size produced by option a) and b) reaches dimensions of the design rules of electronic devices (~0.2 μm) it is necessary to reduce the bulk defects below the critical sub micron dimensions. This approach leads to the development of so called defect free/perfect silicon. The perfect suitability for present and future device generations is achieved by a drastic reduction of the density of vacancies and interstitial type defects in parallel with a size reduction of the remaining point defects. This is achieved by avoiding intrinsic bulk point defect clustering into extended defects due to modifications during crystal growth. Wafers produced by this approach show GOI values in the 100% range, comparable to epitaxial wafers, and excellent LPD/LLSs values. Typical approaches, which are chosen to realize these products, are:

- pulling crystal very close to thermal equilibrium by v/G(r) –homogenization
- use of intrinsic point defect diffusion and mutual annihilation, e.g. active post heating during CZ growth
- building-in extrinsic sinks or recombination center for intrinsic point defect gettering e.g. nitrogen Co-doping [4]
- performing near wafer surface modifications/healing by high temperature wafer treatment e.g. Hydrogen and/or Argon annealing [5]
- to apply epitaxial layers on top of the wafer surface

Option d): Oxygen precipitation in bulk silicon has advantageous effects in terms of trapping metallic impurities away from the active device regions of the integrated circuits. However near the active region a suppression of the oxygen precipitation is preferable to prevent junction leakage current problems. This has lead to the development of intrinsic gettering heat treatment, which produces a denuded zone near the wafer surface and oxygen precipitates for metal impurity gettering in the bulk of the wafer. Today a clear trend can be observed that more advanced device applications go hand in hand with a reduction of the average oxygen concentration which questions the ability for metallic impurity gettering. Another important factor which influences the oxygen precipitation is the trend toward lower process temperatures and shorter process times in the IC device lines which do not generate a sufficient oxygen precipitation depth profile. This development led to a new set of 200 mm wafer products, which are described in chapter 2.5. It deals with the control of oxygen precipitation and denuded zone formation for internal gettering.

2.2. *Wafer size transition from 200 mm to 300 mm*

The effort to perfect the bulk silicon ingots has been discussed above. Furthermore, the continually increasing chip areas force chip makers into larger wafer diameters to achieve more chips per processed wafer (100-piece rule). Previous estimates show that by the transition from 200mm to 300mm wafer diameter, a cost reduction of 20 to 30 % per produced circuit should be possible [6]. The introduction of 300 mm wafers is admittedly delayed because the 200 mm wafer selling prices have been depressed so dramatically. The originally estimated cost savings for the transition from 200 mm to 300 mm wafers are no longer valid.

It is an established fact in the industry that a transition to a new wafer diameter only makes sense economically, if at least twice the Silicon area per wafer can be utilized. Therefore in the SIA-ITRS Roadmap the following diameter changes are laid out:

Year (Start up Mass production)	1990	2001	2009	2015
Wafer Diameter (mm)	200	300	450	675
Wafer Area (cm^2)	314	707	1590	3579
First Design rule (nm)	800	130	35	25

Table 2: Introduction of new Wafer Diameter

Typically the introduction of a new wafer diameter is handled within one design rule generation: while a production line is running stable with the current design rule generation and wafer diameter, the transition to a new diameter is performed without a change in design rule (Window of Transition Opportunity). Originally the transition from the 200mm to 300mm wafer generation was planned to take place at the 180 nm design rule in 1999. Due to the economic situation of the microelectronics industry and the faster than previously expected advances in design rule reduction, the window of transition opportunity has shifted to the next design rule generation of 130 nm, which corresponds to the start of introduction of 300 mm wafers into mass production in the year 2001

2.3. *Tighter flatness requirements due to the decreasing design rules*

Following the decrease in design rule, resolution in lithography has to be increased which renders a reduction in the exposure wavelength as absolutely necessary. The roadmap in optical lithography over the next few years is given by [7]: KrF with an exposure wavelength at 248 nm enables us down to the 150-130 nm design rule generation. ArF with an exposure wavelength of 193 nm will extend capabilities down to the 130-100 nm design rule generation. F_2 with an exposure wavelength of 157 nm should reach of the 100-70 nm design rule generation.

For the post optical lithography era below the 70 nm design rule x-ray, scalpel, ion-beam projection, extreme and vacuum UV as well as e-beam direct writing techniques are currently under investigation, though scalpel and EUV are the front runners.

In optical lithography, the reduction of the exposure wavelength goes in parallel with a reduction of the depth of focus (DOF) during exposure. This enforces tighter local site flatness values (SFQR) at the wafer surface. The rule of thumb for optical lithography is:

(SFQR) = (0,8.....1,0) * design rule (Eq. 1)

To realize these stringent local flatness requirements, improved and new techniques for "global" wafer shaping like simultaneous double side grinding, advanced Single Side Polishing (SSP), simultaneous Double Side Polishing (DSP) as well as new technologies for "local" flatness improvement like Plasma Assisted Chemical Etching (PACE) are being tested and are under evaluation.

2.4. Reduction in size and density of LPDs / LLSs on the wafer surface

The demand for reduction of size and density of Localized Light Scattering Defects (LPDs/LLS) at the wafer surface is also a consequence of the reduction in the design rule. To avoid yield losses of ULSI circuits due to wafer defects, a single defect at the wafer surface must not exceed $^1/_2$ to $^1/_3$ of the smallest structure size. Therefore the rule:

(min LPD diameter) = (0,3.....0,5) * design rule (Eq. 2)

is applied.

Likewise, the density of LPDs follows the rule:

(max LPD density) = (0,1..0,2) * 1/(max chip area) (Eq. 3a)

or

(max LPD density(1/cm²)) = (6..10) * 10^{-6} *(design rule (nm))² (Eq. 3b)

The maximum tolerable disturbances at the wafer surface depend on size of the design rule and in density of the maximum chip area that will be applied to the wafers. In numerous experiments and investigations it has been found that below a LPD/LLS size of 0.2 µm, intrinsic silicon bulk defects, generated during CZ crystal pulling play a dominant role in the formation of LPDs/LLSs at the wafer surface (see chapter 2.1). Many research activities currently aim for the optimization of crystal growth behavior, temperature distributions and cooling procedures to reduce intrinsic bulk defect density to a minimum and to grow defect free/perfect bulk silicon [8, 9, 10].

2.5. *Introduction of new 200 mm wafer types*

In the late stage of the 200 mm wafer technology, many new wafer types are appearing. These include: defect free/perfect silicon wafers, magic denuded zone (MDZ) wafers, Nitrogen co-doped wafers, Hydrogen/Argon annealed wafer, precipitation tuned (PT), GOI tuned (GT) wafers, etc. These new wafer types are primarily driven by the increasing demand of handheld consumer devices. This application requires high integration density and high-speed performance at lowest power consumption and very strict standby power limitations in addition to the very low costs. The technical requirements drive the decrease in gate oxide thickness, which prompts an increase in leakage current, and as a result of this high standby power consumption. These conflicting facts drive the development of defect free/perfect bulk silicon or defect free zones near the wafer surfaces. This approach extends the polished wafer life cycle. Epitaxial wafers have been considered for these applications, but due to cost reasons they are not actively further investigated. To cope with this situation, two approaches are currently under evaluation:

- Development of silicon ingots, free of clustered point defects into extended defects by modifications in the CZ crystal growing process

- Individual wafer heat and/or annealing steps to modify the near wafer surface region

The first option has been discussed in length in chapter 2.1. Now the second option, the individual wafer heat treatment process to form a defect free /perfect near surface region will be analyzed. The introduction of the magic denuded zone wafer [11] has started this development direction. Using a high temperature RTA treatment, wafers can be produced with reproducible denuded zone depths of about 50 µm. The remaining bulk wafer shows the required precipitate density and therefore sufficient intrinsic gettering properties.

However, there are limitations of this approach. The introduced point defect profile is not very stable due to the high diffusivity of the species. If the device process has adverse temperature/ time conditions in the first process steps, the profile will vanish before the generation of the BMDs take place. These instability problems have been addressed by process modifications. A high temperature RTA step is followed by a low temperature nucleation step which fixes and determines the oxygen precipitate nuclei profile. Only this process combination generates the required stable oxygen precipitate nuclei profile. By this process combination, the precipitation occurs only in the bulk of the wafers and the near surface area is kept precipitate free. With this second precipitate nuclei formation step, the precipitation behavior of the wafer can be tuned or tailored toward the temperature/time conditions of the follow on LSI/VLSI device processes. This addition degree of freedom opens the potential to design high yielding wafers for the respective device lines. This product is introduced as a precipitation tuned (PT) wafer in the silicon industry.

2.6. *Appearance of advanced epi products such as fLASH epi-Wafer*

All of the above described issues with the properties of the bulk silicon can be overcome with the use of epitaxial wafers. The main advantage of epi wafers is that there are no vacancy or

interstitial type defects in the near surface region close to the active devices. Consequently, epi wafers do have very high gate oxide integrity and therefore show highest device yields. However, due to price constraints this product does not have a high acceptance in the market place for applications which are under extreme price pressure. Nevertheless, p/p- and p/p+ wafers are in many device lines for the 0.25/0.18 μm design rule generations and below. Much research work is dedicated to reduce the manufacturing cost of epi wafers while keeping the performance advantages. A very promising approach is the fLASH epi wafer. The cost optimization process starts with the selection of an optimized epi-substrate where lower cost, low LPD/LLS performance (> 0,12 μm) and enhanced oxygen precipitation are important selection criteria. This follows a modified wafering process sequence and a fast thin film epi deposition process with steep temperature ramps and short processing times. Excellent performance in terms of GOI, gettering, LPD/LLS, etc. could been demonstrated. The cost saving potential is close to 20 % of a conventional epitaxial wafer. With this approach the gap between a conventional polished and epitaxial wafer is reduced. The fLASH epi wafer is a cost attractive alternative to the new high performance polished wafer as described in chapter 2.5.

2.7. Changing Market Conditions

The technological challenges of the silicon industry have been treated in depth, but there are additional challenges in this industry. First class product quality and a competitive price are basic requirements that allow customer-vendor-relationships to work smoothly. Increasingly, logistic factors are gaining importance and start to rule competition. Flexibility and on-time delivery as well as the highest possible speed in every respect are decisive criteria today for placing an order. The wafer vendor is part of a complete supply chain and must react to customer requirements as fast as possible. The drivers of these changes are:

- Increased global competition
- Integrated Supply chain management in phase with customers demand
- Treatment of small wafer diameter products as commodities
- Growth of electronic commerce (e-commerce)
- SPC data exchange via Internet prior to the product delivery
- Utmost flexible response to customers expectations in the areas of cost reduction and customization of the wafer product to customers needs
- Significant reduction in cycle time and lead-time
- Elimination of inventories
- Unreliable demand / supply forecasts due to rapidly changing market conditions
- Growing risk of not utilizing installed production capacities

All these technological and logistical challenges in the silicon wafer industry are summarized in a very simple formula: much better, much faster, much cheaper and not predictable.

2.8. Extreme cost constraints

Price erosions of 25 % per year at 200 mm wafers occurred in 1997 and again in 1998. As a consequence, the pressure to reduce manufacturing costs of the silicon wafer constantly

increases. This dramatic collapse in revenue can only be absorbed, if at all, by radical process simplification, standardization and extreme cost awareness at all steps.

3. *Summary and Outlook*

As the Semiconductor industry moves into the 21st century, the challenges for the wafer supplier have been analyzed and the different developments which attempt to master these challenges have been investigated. It is evident that the CZ-crystal pulling process is pressured by most of the challenges with respect to perfection of bulk crystals, large diameter ingots and economical price constraints. These CZ activities are followed by new approaches for wafer surface preparation methodologies to improve wafer flatness and LPD/LLS values as well as new RTA/heat treatments to tune the wafer device performance towards LSI/VLSI device line needs. New, high resolution inspection metrology techniques and analytical tools with lower detection limits are urgently needed to support these development activities. In these fields a lot of research work still needs to be done

4. *Acknowledgments*

The author is obliged to the Wacker personnel C. Höss, H. Ölkrug, W. v.Ammon, B. Rexer, A. Schnegg, K. Röttger, G. Wenski, J. Vanhellemont, G. Obermeier, J. Hage, D. Gräf, J. Moreland, H. Fusstetter, and P. Stallhofer as well as different other colleagues for the discussion and valuable comments to this article. The suggestions and recommendations from the university institutes are highly appreciated. The Federal Ministry of Education, Science and Technology of Germany have supported part of this work.

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