Intrinsic Point Defects and Their Control in Silicon Crystal Growth and Wafer Processing

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Introduction

Silicon produced for the microelectronics industry is far and away the purest and most perfect crystalline material manufactured today. It is fabricated routinely and in very large volumes. Many of the advances in integrated-circuit (IC) manufacturing achieved in recent years would not have been possible without parallel advances in silicon-crystal quality and defect engineering. Transition-metal contamination is a case in point. Essentially all practical problems (minority carrier lifetime, metal precipitation, stacking faults, etc.) associated with metal contaminants have largely been solved through advances in crystal purity.

Today, silicon technology faces two main defect challenges, neither of which can be solved simply by increasing the level of crystal *purity*, as was the case in the transition-metal problem. So important are these problems that they in fact challenge the very status of the traditional, polished, Czochralski-grown silicon wafer (as opposed to the much costlier epitaxial silicon substrate) as a suitable material for the coming generations of advanced IC processes. One of these challenges arises from the *intrinsic*, or *native*, point defects, lattice vacancies, and silicon self-interstitials, and the other from the most important *extrinsic* point defect in Czochralski-grown silicon: oxygen. Large advances have been made recently in these areas, producing solutions to these engineering problems. Although the solutions to these two problems are completely separate (one is imposed on the crystal-growth process and the other on wafer heat-treating), they are related; the underlying science is shared by both and is common to the range of topics covered in this issue. In particular, studies of point defects from the point of view of crystal growth and oxygen-precipitation control can give new insights into the elusive properties of these defects. This article summarizes these advances in silicon science and engineering.

Vacancies and Interstitials and Their Agglomerates in Silicon Crystals

Microdefects in silicon related to intrinsic point defects were first observed in the early 1960s—ironically, almost immediately after the main silicon-crystal problem of the day was solved, that of dislocation-free growth. Eliminating dislocations from silicon crystals simultaneously eliminated an important distributed sink for "grown-in" intrinsic point defects, thus allowing them to homogeneously agglomerate. One problem solved, another created. It was not, however, until recent years that demands for crystal perfection reached such extremes that specific problems associated with these defect types were identified, and urgent solutions were demanded.

The study of these microdefect agglomerates and their related effects on crystal growth has yielded a rich array of information on the properties of intrinsic point defects at high temperatures. The incorporation of intrinsic point defects into a growing crystal and their subsequent agglomeration into larger defects are controlled by the details of how the crystal is solidified and subsequently cooled.

Interstitial- and vacancy-type microdefects occur in two clearly defined modes of growth. A threshold (or critical) growth rate (v_{cr}) for a changeover from interstitial-type defects (A/B swirl defects) to vacancy-type ("D") defects exists and was found to be proportional to the near-interface axial temperature gradient G.[1,2] In other words, the type of grown-in microdefects is controlled simply by the ratio v/G. Swirl defects are formed if v/G is below some universal critical ratio ξ_t, and D defects are formed otherwise. This simple and important "v/G rule" holds both for float-zone and Czochralski-grown crystals,[3] in spite of a great difference in the oxygen content. The physical meaning of this rule is very simple:[1] the type of intrinsic point defect incorporated into a growing crystal is controlled by the parameter v/G, according to the defect transport equations for diffusion, convection, and annihilation of point defects in the vicinity of the interface.

Vacancy Growth Mode

Growing a crystal at $v/G > \xi_t$ results in the incorporation of vacancies while the interstitial concentration is undersaturated, and it decays quickly due to recombination with vacancies. The vacancies agglomerate into voids (D defects) on further cooling if the vacancy concentration is not too low.[3] The identification of D defects as octahedral voids was recently demonstrated.[4,5] The voids, although they are of low density (ca. 10^6 cm^{-3}) and small size (ca. 150 nm), can cause large yield problems in the manufacture of some high-density ICs, in particular, dynamic random-access memory (DRAM) chips. The main problem is a gate oxide failure, which can result from the intersection of such a void with the polished silicon surface. Other void-related problems are encountered in device isolation.[6]

At a low vacancy concentration, void formation is suppressed, and instead, oxide particles are produced from a supersaturated vacancy solution.[3] At a still-lower vacancy concentration, even the vacancy consumption is suppressed, with the consequence of an appreciable residual vacancy concentration, which can greatly increase oxygen precipitation.[7,8] For these reasons, the main vacancy region (containing voids) is surrounded first by a marginal particle band (P-band) and further by a band of enhanced oxygen precipitation (L-band). Particularly, the P-band is often manifested as a so-called

OSF (oxidation-induced stacking fault) ring in oxidized wafers.

Figure 1 is a kind of vacancy "map" that illustrates the problem of incorporating vacancies into a growing crystal. Starting at the equilibrium vacancy concentration at the melt temperature, $C_V^{eq}(T_m)$, the vacancy concentration is reduced as the crystal cools through a transient phase in which vacancy and self-interstitial fluxes compete with each other by means of mutual annihilation. Eventually this stops when the concentration of self-interstitials is exhausted. At this point, an essentially constant concentration of the surviving species (vacancy) is obtained. It is the surviving vacancy concentration, set at high temperature by the v/G rule, that is then launched into the possible reactions at lower temperatures. The reference value of the ratio of the actual to critical v/G value is given on the right-hand scale in Figure 1 for several examples.

Interstitial Growth Mode

Growing a crystal at $v/G < \xi_t$ results in the incorporation of self-interstitials while the vacancy concentration is undersaturated, and it decays rapidly. The resulting supersaturated self-interstitials agglomerate into A/B swirl defects. The A defects were found to be extrinsic dislocation loops;[9] these are considered to be even more dangerous microdefects than voids. The B defects seem to be small, globular clusters of interstitials[10] (most likely including carbon interstitials). Particularly at a low interstitial concentration, only B defects are formed. At still-lower concentrations, no *detectable* defects are formed. Accordingly, the main interstitial region of a crystal (the region containing A defects) is surrounded by a band of B defects.

An example of the richness of defect distribution possible in a silicon crystal is shown in Figure 2. This image and the defect map were obtained from a crystal grown with a decreasing pull rate to switch the growth condition from the vacancy to the interstitial growth mode.

Void-Reaction Control

One approach to an engineering improvement of the microdefect problem is to grow crystals in the vacancy mode, while engineering the reactions that produce voids. The resultant density of voids is proportional to the factor $q^{3/2}C_V^{-1/2}$,[3] where q is the cooling rate at the temperature at which the reaction occurs, and C_V is the local concentration of vacancies (a function of v/G). The void reaction occurs over a very narrow temperature range ($\Delta T \sim 5$ K) at some "nucleation temperature," T_{nuc}, that depends on C_V.[3] The range of T_{nuc} lies between about 1000°C and 1100°C.[7,11,12] Figure 3 shows an example of the path taken by vacancies through void formation and subsequent vacancy consumption for a specific v/G condition.

The problem of reducing void-defect density is thus a coupled engineering problem. One must engineer simultaneously the coupled problems of the incorporation of vacancies near the growth interface (v and G at about the melt temperature) and the cooling rate at the reaction temperature (v and G at a temperature that depends on C_V). This can be done by decreasing G to around 1100°C, but for largely practical reasons, only about a 10× reduction in void density is possible. For some applications, this is not enough improvement to ensure device yields that are not limited by the starting substrate defectivity.

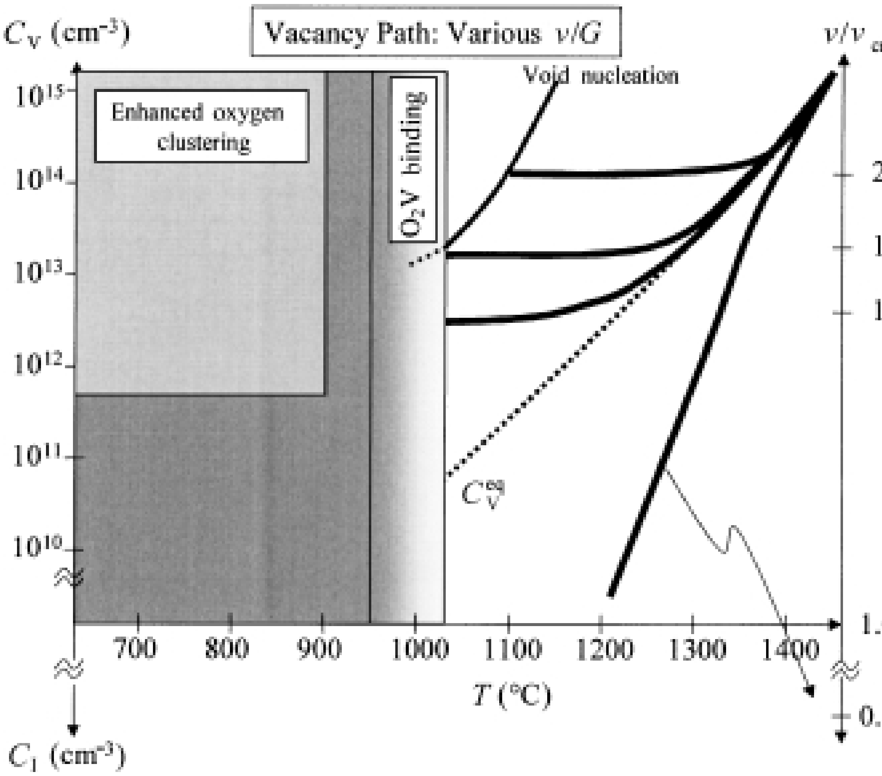

Figure 1. An illustration of the incorporation of vacancies into a growing crystal. Bold solid curves show the evolution of the dissolved vacancy concentration C_V during cooling of the crystal for four values of v/v_{cr} (where $v_{cr} = G\xi_t$). The thinner solid curve represents the void nucleation temperature T_{nuc} as a function of C_V. V stands for vacancy, v is the crystal growth rate, v_{cr} is the critical growth rate at which interstitial-type defects change over to vacancy-type defects, G is the near-interface axial temperature gradient, and ξ_t is a universal critical ratio below which A/B swirl defects form.

Perfect Silicon

A more robust solution to the microdefect problem, and one that circumvents the question and resultant complications of whether the material is sufficiently improved to meet the needs of an arbitrary IC process, is not to control the microdefect reaction, but rather to suppress it. As described in the earlier section on "Vacancy Growth Mode," there are two marginal bands straddling the transition from vacancy- to interstitial-type silicon in which the reactions that produce microdefects do not occur. In these regions, the concentrations of either vacancies or self-interstitials are too low to drive the reactions during the cooling of the crystal. They differ in character due to the differing effects of unreacted vacancies or interstitials on the subsequent nucleation of oxygen clusters at lower temperatures. Excess vacancies enhance the clustering, while excess interstitials suppress it. In terms of process control, the width in v/G space around the critical value that produces sufficiently low concentrations of either vacancies or interstitials is of the order of 10%. Growth processes that can control v/G to within 10% around the critical value both axially and radially are capable of producing microdefect-free silicon. This is not an easy task. Methods

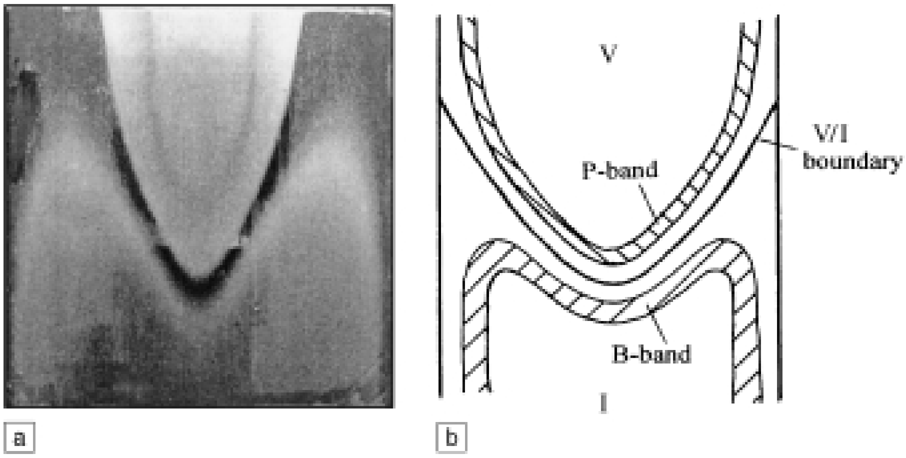

Figure 2. (a) An axial cross section of an etched Cu-decorated (150-nm diameter) Czochralski-grown crystal at the transition from vacancy-type defect growth conditions (the upper U-shaped section) and interstitial-type defect conditions (the lower M-shaped structure). (b) A schematic diagram of the structure.

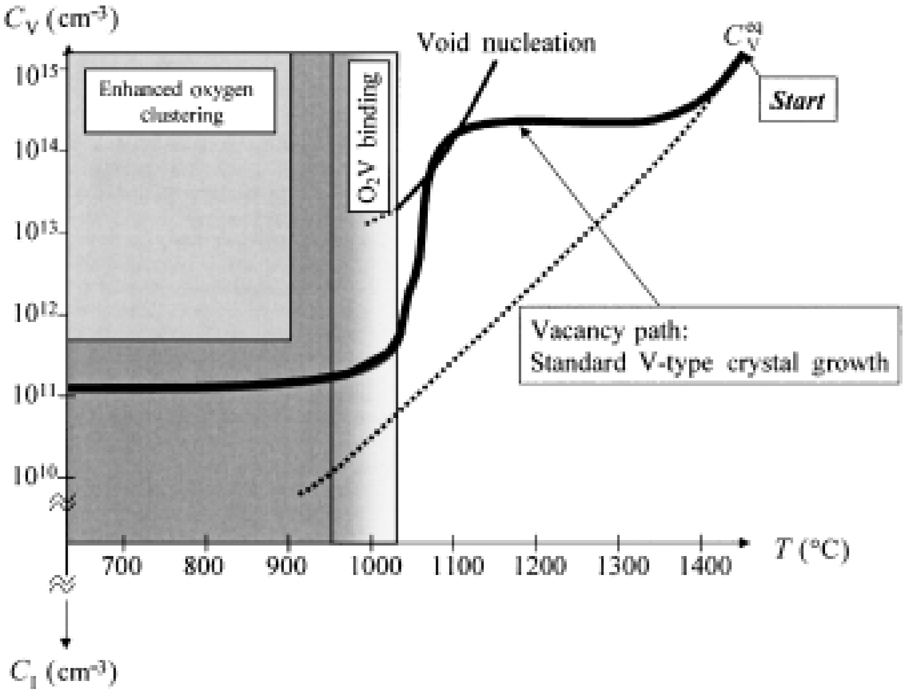

Figure 3. An illustration of the production of voids in a growing crystal in the most usual case.

exist that result in the partial relaxation of this requirement, such that the production of such "perfect silicon" is practically possible along nearly the entire crystal length.

The "Magic Denuded Zone" Wafer

The Control of Oxygen Precipitation and its Impact on Internal Gettering

The control of the behavior of oxygen in silicon is undeniably one of the most important challenges in semiconductor materials engineering. In particular, control of oxygen precipitation is essential for the development of internal gettering (IG) in IC manufacturing, as described in the article by Istratov et al. in this issue. Such gettering schemes play an important role in yield management in IC manufacturing. In the 20 or so years since the discovery of the IG effect in silicon wafers, many scientists and engineers have struggled with the problem of precisely and reliably controlling the precipitation of oxygen that occurs in silicon during the processing of wafers into integrated circuits. This has met with only partial success, in the sense that the "defect engineering" of conventional silicon wafers is still, by and large, an *empirical* exercise. It consists largely of careful, empirical tailoring of wafer type (oxygen concentration, crystal-growth method, and details of any additional pre-heat treatments, for example) to match the *specific* process details of the application to which the wafers are submitted, in order to achieve good *and* reliable IG performance. Reliable and efficient IG requires the robust formation of oxygen-precipitate-free surface regions ("denuded zones") and a bulk defective layer consisting of a minimum density[13] (at least about $10^8\,\mathrm{cm}^{-3}$) of oxygen precipitates during the processing of the silicon wafer. Uncontrolled precipitation of oxygen in the near-surface region of the wafer represents a risk to device yield. The basis of the conventional method for dealing with the creation of such a layered structure has been to ensure sufficient out-diffusion of oxygen from the near-surface region in order to suppress nucleation and growth. In recent years, due to radical reductions in the total thermal budgets of processes that make submicron devices, this is no longer possible, except at a large added cost.

Vacancy-Controlled Oxygen Precipitation

But there is another way.[14] In the previous discussion of vacancy incorporation in crystal growth, we noted that there is a region of vacancy concentration accessible through crystal growth in which no microdefects are formed, yet clustering of oxygen is significantly enhanced. It is also possible to achieve such levels of vacancy concentration *after* growth in *thin* wafers through the proper control of their heating and cooling. In fact, it is possible, through the judicious control of point-defect generation, injection, diffusion, and recombination, to install vacancy-concentration profiles into silicon wafers that result in the ideal precipitation performance for IG purposes. Such an ideal vacancy profile means a high vacancy concentration in the wafer bulk and proper vacancy depletion in the near-surface region. The installation of controlled concentration profiles of vacancies is now a wafer-manufacturing process.

While a high concentration of vacancies enhances oxygen clustering, there is a lower bound on vacancy concentration below which clustering is "normal." This is quite a sharp transition and lies around

5×10^{11} cm^{-3}. Thus a profiled vacancy concentration allows for the programming of “layered” structures, just what is required for the effective engineering of structures by IG. This is the basis underlying the “Magic Denuded Zone”(or MDZ) wafer.[14] A schematic illustration of this new materials-processing technique is shown in Figure 4. The use of such a *vacancy-based* approach greatly simplifies the use of silicon by decoupling the formation of the IG structure from the details of the crystal-growth process, the oxygen content of the wafer, and the details of the thermal process used to fabricate the device in question.

The Installation of Vacancy-Concentration Profiles in Thin Silicon Wafers

The installation of appropriate vacancy-concentration profiles in thin silicon wafers is a three-step process, but all steps occur in a single rapid thermal processing (RTP) run.[14]

1. When silicon is raised to high temperatures, vacancies and interstitials are spontaneously produced in equal amounts through Frenkel pair generation, a very fast reaction. At distances far removed from crystal surfaces, we thus have $C_I = C_V = \{C_I^{eq}(T)C_V^{eq}(T)\}^{1/2}$, where T is the process temperature. If the sample were to be cooled at this point, the vacancies and interstitials would merely mutually annihilate each other in the reverse process of their generation.

2. In thin wafers, however, the surfaces are not far away, and this situation changes very rapidly. Equilibrium boundary conditions (not oxidizing or nitriding) lead to coupled fluxes of interstitials to the surface and vacancies from the surface because $C_I^{eq}(T) < C_V^{eq}(T)$, and because of the rapid establishment of equilibrium conditions throughout the thickness of the wafer. Experiments suggest that this occurs very rapidly—in a matter of seconds or less. This equilibration is primarily controlled by the diffusivity of the fastest component, the self-interstitials, since the concentrations are roughly equal.

3. Upon cooling, two processes are important: direct recombination of vacancies and interstitials, and diffusion of interstitials toward the surfaces. In the wafer bulk, the slower vacancies are now the dominant species of the coupled diffusion, and hence the equilibration process at the surface is not as fast as the interstitial-dominated initial equilibration. It is thus possible to “freeze-in” excess bulk vacancies at not-unreasonable cooling rates (ca. 50–100°C / s). The residual bulk concentration of vacancies following recombination with interstitials, C_V, is the initial difference of $C_V^{eq} - C_I^{eq}$ (at the process temperature T). Closer to the surfaces, C_V is lower, due to out-diffusion (again, primarily controlled by the dominant vacancies) toward the decreasing equilibrium values at the wafer surface. The level of bulk precipitation is controlled by the process temperature, through $C_V^{eq} - C_I^{eq}$, while the depth of the denuded zone is controlled by the cooling rate, through the diffusion of vacancies during cooling. Such information, coupled with numerical simulation of the diffusion process, can provide very important points of reference in analyzing the parameters of the native point defects in silicon. For example, the difference in the equilibrium concentrations, $C_V^{eq} - C_I^{eq}$, is $5–8 \times 10^{11}$ cm^{-3} at about 1175°C, while at about 1250°C, a much higher value is found, about $2–5 \times 10^{12}$ cm^{-3}. Further experiments with various cooling rates and subsequent relaxation rates of an installed profile during a second RTP process at a different temperature give insight into the diffusivity of vacancies at various temperatures. Information gained from such experiments can be coupled with information gleaned from crystal-growth experiments to compile a unified picture of the point-defect parameters at high temperatures.[15] The rules governing vacancy-interstitial reactions and diffusion are the same for wafer processing as for crystal growth. Figure 5 shows a schematic diagram of the installation of vacancy-concentration profiles by RTP of thin wafers in the same format as that used to describe crystal reactions.

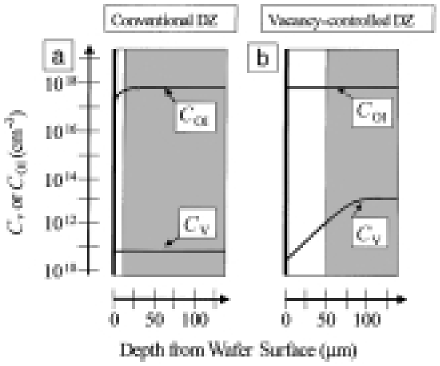

Figure 4. Schematic comparison of (a) conventional and (b) vacancy-controlled denuded zones (DZs). The shaded regions are those of subsequent high levels of oxygen precipitation. C_{OI} and C_V are interstitial-oxygen and vacancy concentrations, respectively.

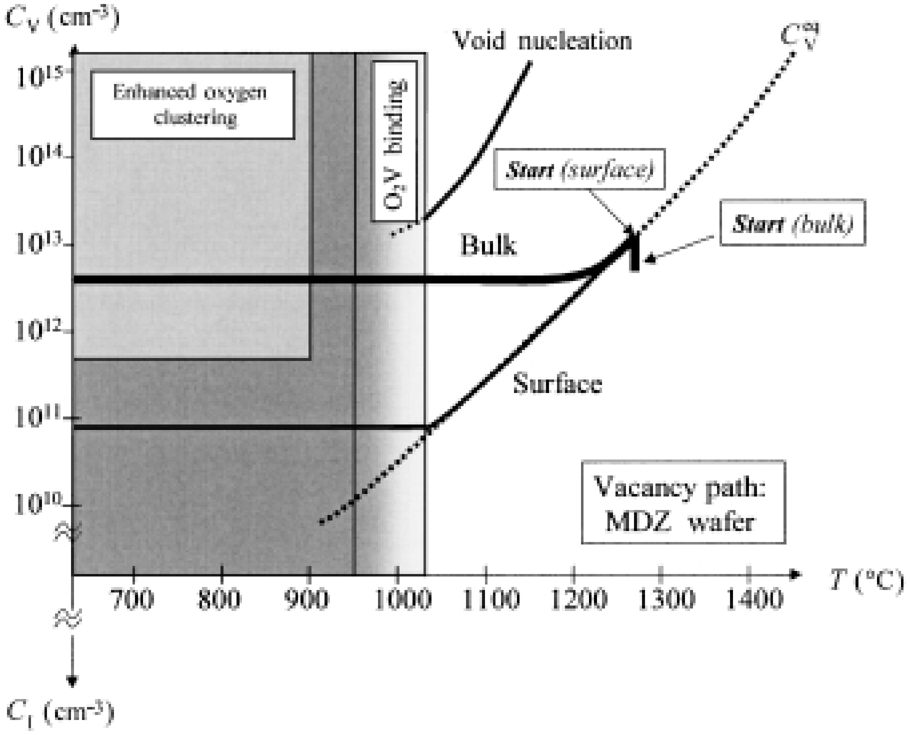

Figure 5. An illustration of the use of the vacancy template to illustrate the creation of layered precipitation effects in thin silicon wafers [the Magic Denuded Zone (MDZ) wafer] by means of high-temperature rapid thermal processing.

Conclusions

A unified picture of point-defect behavior can be derived from the data on grown-in microdefects and the vacancy profiles created in wafers by rapid thermal processing. The basic points are

1. The equilibrium vacancy concentration is slightly higher than that of self-interstitials, at least at temperatures over 1150°C. This basic inequality allows for (a) vacancy incorporation into the growing crystal at v/G over some critical value and (b) installation of a vacancy profile in RTP-treated wafers to ensure MDZ formation.
2. The interstitial diffusivity is essentially higher than that of vacancies. As a consequence of this inequality, (a) the self-interstitials are incorporated into the growing crystal at low v/G when the diffusion becomes more important than convection; and (b) equilibration of point-defect profiles is very fast at the RTP temperature, but not as fast during subsequent cooling, to ensure the desired installed profile of vacancies.
3. The recombination rate of vacancies and interstitials is very fast at $T > 1150$°C. This condition is equally important, both in defect incorporation during growth (to account for the v/G rule) and in fast installation of the vacancy profile in wafers.

Information derived from the relatively simple intrinsic cases investigated here (high temperatures and unbound vacancies) are of importance to the other point-defect areas covered in the accompanying articles in this issue.

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