Anodic etching of *p*-type silicon as a method for discriminating electrically active and inactive defects

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Anodic etching of defects in *p*-type Si can be achieved at small applied voltages with dilute HF as electrolyte. The etching behavior of defects is strongly voltage dependent. At very small voltages only electrically active defects are etched; this is shown by comparison to EBIC. At higher voltages all defects are etched. The method provides a unique tool for investigating geometrical, structural, *and* electronic properties of defects in a simple way and offers considerable advantages over conventional techniques.

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A quick and simple method for revealing defects in silicon is essential in relation to many of its device applications. Information about geometry, structure, and electronic properties of defects is commonly needed and the methods mostly used to obtain these data are preferential chemical etching,[1–3] for geometry and structure, and scanning electron microscopy in the electron-beam-induced current mode (EBIC),[4] for electronic properties. Chemical etching, although simple in application, suffers from a lack of basic understanding. It is often difficult to predict how a particular specimen will respond to a given etch and frequently some doubts remain as to whether a certain etch did reveal all defects, only specific defects, or even produced artifact structures. EBIC, on the other hand, is well understood, but a scanning microscope and involved specimen preparation techniques are needed, and it can be applied only to small areas of a specimen.

This letter reports the application to *p*-type Si of a new technique which gives information concerning electronic properties of defects (as in EBIC) and their geometrical and structural characteristics. The method is electrochemical in nature and is almost as easy to use as chemical etching but is less hazardous since no concentrated acids are involved. Depending on the voltage applied to the electrochemical cell, only electrically active defects, or all defects can be etched. This letter gives a first account of the technique; a detailed study is presented elsewhere.[5]

The *p*-type Si under investigation is biased as the anode in an electrochemical cell consisting of a Pt wire as cathode and dilute HF (typically to 5%) as electrolyte. Dilution with a 1:1 mixture of H_2O and ethanol makes etching more uniform than dilution with water alone. The open-circuit cell voltage is about 0.7 V (the Si electrode being the positive terminal) and the applied voltages ranged from −0.7 (re-

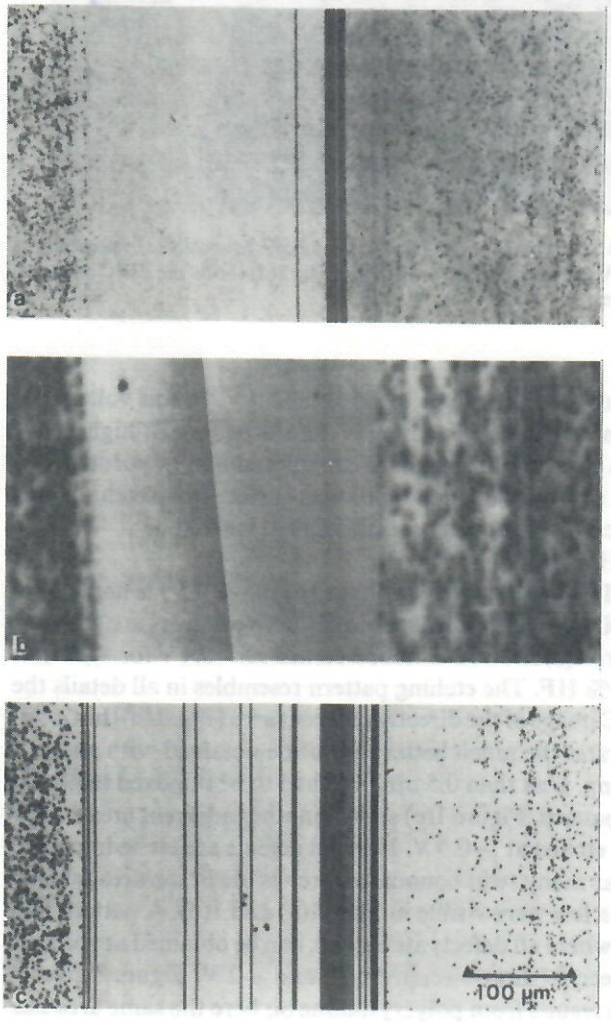

FIG. 1 (a) Silicon ribbon anodically etched at −0.4 V, (b) EBIC image of adjacent area, (c) adjacent area anodically etched at +0.4 V.

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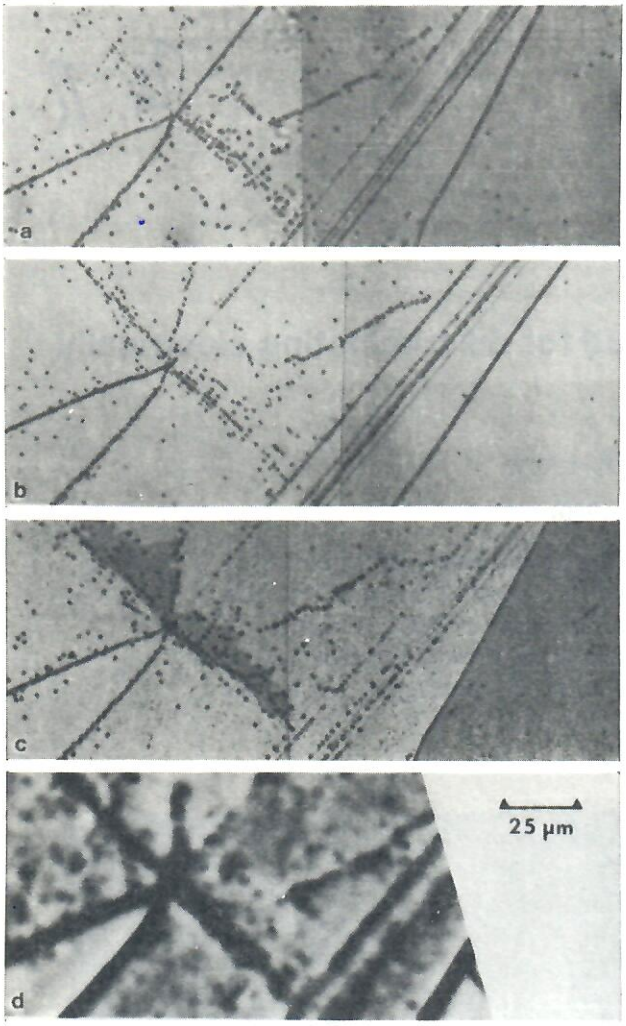

FIG. 2 Same area in polycrystalline Si etched, chemically (a), anodically at +0.4 V (b), anodically at −0.4 V (c); Fig. 2(d) shows the EBIC image of this area.

ducing the cell voltage to zero) to $\gtrsim 5$ V. In this voltage regime preferential etching of defects occurs; at higher voltages electropolishing starts. A colored film of porous Si (Ref. 6) is formed on the specimen surface upon etching; this film can be removed by a subsequent treatment at ~7 V in 1% HF solution.

If a small negative voltage (e.g., −0.4 V) is applied to the Si electrode, only electrically active defects are etched. Figure 1(a) shows a Si ribbon etched at −0.4 V for ~20 min in 10% HF. The etching pattern resembles in all details the EBIC image of the directly adjacent area [Fig. 1(b)] but demonstrates the much better resolution obtained with anodic etching. Less than 0.5 μm of Si had to be removed to obtain this pattern. Figure 1(c) shows another adjacent area anodically etched at +0.5 V. Here all defects are etched; in particular many twin boundaries are visible in the area where only a few were visible in Figs. 1(a) and 1(b). A pattern like this, where all defects are etched, can be obtained at voltages between 0 (short-circuited cell) and ~2 V. Figure 2 gives some results from polycrystalline Si; here the same area has been investigated by Sirtl etching[1] [Fig. 2(a)], anodic etching at +0.4 V [Fig. 2(b)], anodic etching at −0.4 V [Fig. 2(c)], and EBIC [Fig. 2(d)]. Again, anodic etching at −0.4 V is very similar to EBIC but exhibits superior resolution. Sirtl etching does not reveal all the twin boundaries present (this was also observed for Secco etching[2]), whereas anodic etching at +0.4 V shows all boundaries.

If the applied voltage is raised above ~2 V, the etched features of defects become less distinct and electropolishing will eventually occur. In an intermediate region (around 5 V), grain boundaries only are revealed; they are located at steps between differently oriented grains indicating that the etching rate remains sensitive to the surface orientation of the Si.

The preferential etching of only electrically active defects at low voltages provides a convenient method to "mark" these defects (by their etch grooves) for subsequent transmission electron microscopy (TEM). Preliminary TEM studies of the twin boundaries in Fig. 1 show that there is no visible difference between the electronically active and inactive defects (which were found to be mostly microtwins). This is an unexpected result since it is generally assumed that electrically active (coherent) twin boundaries would contain secondary defects such as dislocation networks.[7]

The electronic behavior of the silicon-electrolyte interface is very similar to that of the silicon-metal interface; its voltage-current characteristic is that of a diode. Since only holes participate in the dissolution process,[6,8] p-type Si is forward biased if a positive voltage is applied and will dissolve readily if the potential is higher than the "threshold" potential of the diode. If a negative voltage is applied to p-type Si, the current is small (reverse-biased diode) and this is also true for n-type Si positively biased. This effect has already been used to etch electronically active defects in n-type semiconductors[9-11] because current will only flow (and etching only occur) in areas where defects can act as generation centers for holes. Since holes are the majority carriers in p-type Si, it was believed that anodic etching of defects in p-type semiconductors was not feasible.[11]

The present results demonstrate that defects in p-type Si can have very pronounced effects on the dissolution rate at voltages corresponding to the threshold voltage in the forward direction of the Si-electrolyte diode. Carrier transfer from undisturbed crystal regions to the electrolyte is prohibited at low voltages owing to band bending near the surface. However, defect states in the band gap may provide carrier transfer possibilities which are absent in the perfect crystal and preferential chemical etching of electrically active defects occurs. Etching of electrically inactive (or weakly active) defects occurs at higher voltages, i.e., under conditions where the etching rate of a perfect crystal is found to be sensitive to its surface orientation. This may indicate that electrically inactive defects can influence the surface conditions although they do not have (bulk) states in the band gap.

Clearly, more work is required before all details of the technique are understood. In particular, measurements are needed of the etching behavior of particular defects as a function of the Si electrode potential (rather than applied voltage), the HF concentration, and the Si resistivity. Besides providing a powerful technique for studying geometrical and electronic properties of defects in semiconductors,

this might ultimately lead to a better understanding of defect properties in general.

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