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Anodic Etching of Defects in P-Type Silicon

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ABSTRACT

A new etching technique for p-type Si has been developed which combines the advantages of chemical etching and EBIC. The method is electrochemical in nature and the silicon sample is biased as the anode in an electrochemical cell. The etching behavior of defects is governed by the magnitude of the applied voltage. At low voltages only electronically active defects are etched and the etching pattern corresponds to an EBIC image of the same area. At higher voltages all defects are etched and the etching behavior resembles chemical etching. The method offers considerable advantages as compared to EBIC and chemical etching.

Preferential chemical etching of defects in Si crystals with special chemical solutions ("etches") has been the most important technique for revealing defects in crystalline Si. An etching solution based on the HF-CrO_3 system which was first introduced by Sirtl and Adler (1) has been widely used in its original form or in modified versions (2-4) but etches based on the HF-HNO_3 system are also used (5, 6).

Despite the widespread use of these etches, it is not understood exactly how they work, *i.e.*, why, under certain circumstances, they attack certain defects with an etching rate different from that of the perfect crystal. This is illustrated, *e.g.*, by the remarkable difference in the etching behavior of the Sirtl-, Secco-, and Seiter-etch (1, 2, 4), all of which are based on the HF-CrO_3 system: whereas Sirtl etch works best on {111} planes and not on {100} planes, the Seiter etch is sensitive to all crystal planes except the {111} plane. Finally, the Secco etch works on all crystal planes.

This lack of universality of most etches is no major drawback for the purpose of defect delineation in single crystals of Si because the crystal orientation and the kinds of defects which might be present usually are known. Thus the proper etch can be chosen and fine-tuned to the specific application without major problems [see Ref. (7) for an example].

The situation has changed with the advent of polycrystalline Si for photovoltaic applications in recent years. Neither the orientation of various grains nor the nature of defects to be expected is known: all kinds of dislocations, stacking faults, low- and high-angle grain boundaries, and precipitates of impurities may be present simultaneously. Application of standard etching procedures thus may leave defects undetected or give different responses in different grains. Moreover, the response of grain boundaries to the various etches is not known.

Key words: etching, dejects, crystals.

Chemical etching gives information about the presence of certain defects, but no information about their electronic activity. Because the latter is the most interesting property of defects with respect to photovoltaics, additional experimental methods such as scanning microscopy in the electron-beam induced current (EBIC) mode have to be employed if electronic properties are to be studied.

This paper proposes a new etching method for p-type silicon which is based on electrochemical methods. It exploits the difference between the electrochemical potential of defects and the silicon matrix. Therefore, etching features can be related to electronic properties of defects. The same information about defects as obtained in EBIC measurements can be derived, making this method especially suited for the evaluation of polycrystalline Si. The method can be easily extended to all kinds of p-type Si crystals and possibly to other semiconductors.

Background: Electrochemistry of Silicon

If Si is anodically biased in an electrochemical cell and a suitable electrolyte is used, it will dissolve with a rate proportional to the current density (8-10). It has been shown that the dissolution process requires holes, therefore only p-type Si will dissolve anodically with ease. The silicon-electrolyte interface behaves in

many respects like a Schottky diode which is forwardly biased for p-type Si and reversely biased for n-type Si. Consequently, even with a rather high voltage applied to the electrochemical cell, n-type Si will not dissolve rapidly and the current density will be small (corresponding to the leakage current of a reversely biased diode). A space-charge region is built up at the Si-electrolyte interface and any defects present in this layer which are able to generate holes, may locally enhance the current density and thus the etching rate. This effect is known to provide a valuable tool for etching "electronically active" defects and has already been mentioned by Turner (8). Anodic etching of n-type GaAs has indeed been used for some time for defect detection and was shown to offer considerable advantages over chemical etching (11-13), but not until recently was it applied to the characterization of defects in n-type Si (14).

Anodic etching of defects in p-type semiconductors has not been attempted so far. Since holes are the majority carriers in this case, no influence of defects on the current density was expected. Moreover, a layer of so-called porous Si (8, 15) is frequently formed on the etched surface and this was believed to mask possible preferential etching of defects (14). While this is true for bias voltages larger than a few volts, it will be shown in this paper that at low bias voltages a very pronounced etching of defects occurs. In this case the silicon half-cell is operated around or below the threshold voltage for current flow in the forward direction (in the diode picture of the half-cell) and the presence of defects can substantially alter the current-voltage characteristic of the Si-electrolyte "diode." Moreover, the etching rate for a given defect is very sensitive to changes in the applied voltage and it is different for defects with different electronic properties. Therefore, by varying the applied voltage it is possible to probe the specimen for defects with different electronic activities.

Experimental

A very simple experimental setup was used for the present work. The electrolytic cell consisted of a plastic beaker, and a Pt wire was used as the cathode of the system. The solution was agitated by a magnetic stirrer and etching was usually performed at room temperature in the dark. No reference electrodes were used and measurements of currents and voltages were made with typical (low impedance) laboratory instruments.

The specimens used were polycrystalline silicon obtained by unidirectional solidification (16) with a resistivity of ~10-20 Ωcm and silicon ribbons (17) with a resistivity of ~1-2 Ωcm. The specimens were mounted on a metal stick and the back side contact was made by a drop of liquid Ga-In alloy. A good back side contact was found to be essential; earlier experiments using carbon- or silver-paste yielded irreproducible results. The specimen holder and the edges of the specimen were then covered with wax so that only the surface of the specimen was exposed to the electrolyte. The electrolyte was HF [49%] diluted with a 50:50 mixture of distilled water and absolute ethanol so that the HF concentration was typically 1-10%. If water alone was used as a dilutant, the etching was often inhomogeneous and spotty in appearance, probably because of wetting problems. A constant voltage power supply was used and the voltage applied ranged from −0.5 to +20V. The small negative voltages still biased the silicon anodically because the built-in voltage of the Pt-Si cell was around 0.7V.

Some of the specimens were subjected to electron-beam induced current (EBIC) measurements in a scanning electron microscope (18). The Schottky contact necessary to apply this technique was made by evaporating 40-50 nm of Ti on the carefully cleaned sample surface.

Results

General observations.—The open-circuit voltage of the Pt-HF [5%]-Si system is about 0.7V; the silicon electrode is the positive terminal of the cell. A typical current-voltage curve is shown in Fig. 1 for poly-Si. Preferential etching of defects can be achieved in the region between −0.7 and ~2V. Figure 2 shows an example to illustrate the etching quality. The poly-Si specimen was etched ~40 min at 0V bias voltage (short-circuited cell); the current density was ~1.3 mA/cm² and ~3 μm of Si was removed during etching. Dislocations and grain boundaries are clearly visible; the dislocation etch pits are usually round or elliptical and can be very extended for dislocations running nearly parallel to the surface. Any surface damage is also revealed because only the top layer of the crystal was removed.

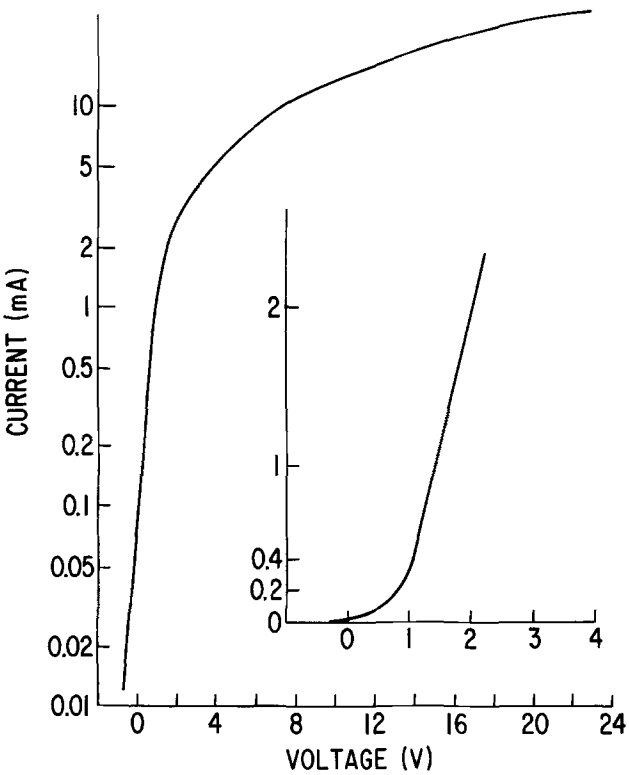

Fig. 1. Current-voltage characteristic for poly-Si in 5% HF. The inset shows the current-voltage characteristic for small voltages on a linear scale.

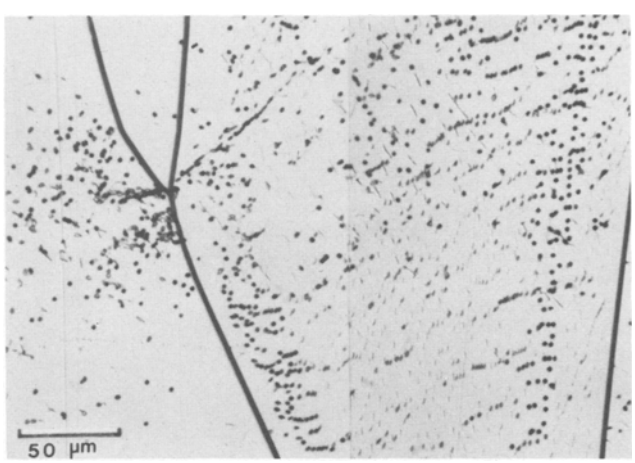

Fig. 2. Example of anodically etched poly-Si (40 min at 0V bias)

If a positive voltage >2V is applied, only grain boundaries are revealed (Fig. 3). If the voltage is further increased, electro-polishing will eventually begin (around 15V, *e.g.*, for poly-Si in a 5% HF solution) and the surface appears to be structureless.

The voltage regions within which these characteristic features are observed depend somewhat on the HF concentration and on the resistivity of the samples. Higher HF concentrations and lower resistivities tend to shift the "critical" voltages to higher values.

It is important to note that grain boundaries may be visible after etching (including purely chemical etching) for two unrelated reasons: they may be preferentially etched, *i.e.*, a groove is formed (Fig. 4a) or they may be outlined as a step between two grains because the etching rate in the two grains was different (Fig. 4b). In general, a mixture between groove and step will prevail (Fig. 4c). It is only when an etch groove is formed that the boundary can be considered to be truly etched. It is not always possible to distinguish between the three cases but a decision can frequently be made if the etch pattern is sufficiently developed and a microscope with interference or Nomarski contrast is used at moderate magnifications (~200-800×).

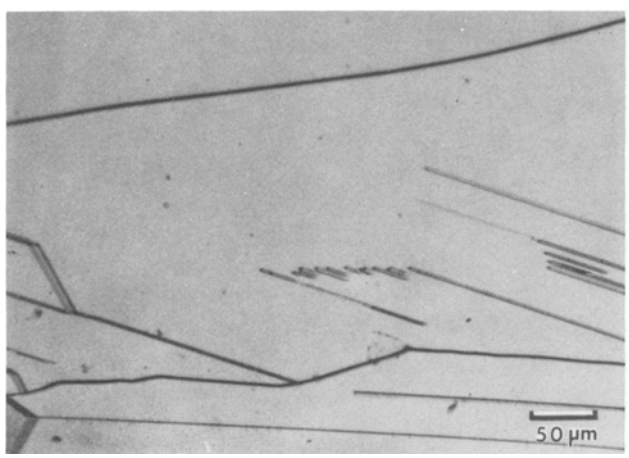

Fig. 3. Example of anodically etched poly-Si (1 min at 5V bias voltage).

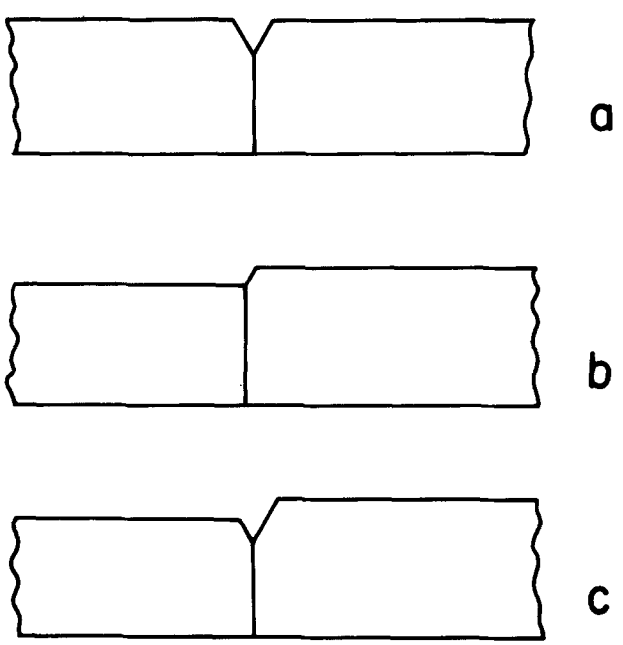

Fig. 4. Schematic outline of possible etching features at grain boundaries.

At low voltages the silicon surface is always covered with a thin layer of so-called porous Si (8, 15). This film mostly appears as a homogeneous layer displaying bright interference colors. Grains with different orientations may be outlined distinctly by this film because they appear in different colors due to a different film thickness. The etch pattern is visible through this film; it is however advantageous to remove it by transferring the specimen to a 1% solution of HF and by applying a voltage of ~7V for 1-2 min. This treatment will always remove the colored layer without changing the etching pattern as has been ascertained in numerous cases. Other methods for removing the porous silicon layer are mentioned in Ref. (15) and may work as well, although they have not been tried in this case. Sometimes, particularly at very low or negative bias voltages, a rough-looking brownish surface appears instead of the colored film. This film could not be completely removed by the above treatment and the surface remains somewhat rough and covered with many small pits. This can be disturbing but does not seriously interfere with the defect etching pattern.

The voltage dependence of preferential etching.— In the low voltage region (−0.7-~2V) the etching behavior of defects is strongly voltage dependent. Figure 5 shows directly neighboring parts of a silicon ribbon etched at 0V (Fig. 5a), −0.4V (Fig. 5b), and +0.5V (Fig. 5c) for 10, 20, and 5 min, respectively. Whereas it is safe to say that the nature and spatial distribution of defects did not change considerably in those parts of the sample probed at the three different voltages, the etching patterns look quite different. Especially if a small negative voltage is applied to the silicon electrode (in order to reduce the open-circuit voltage) many of the (twin) boundaries which were etched at 0 and +0.5V are no longer revealed. Dislocations, however, are still preferentially etched and their density and distribution in Fig. 5b corresponds perfectly to those in Fig. 5a and c. Etching at 0 and +0.5V produces similar patterns but dislocations running nearly parallel to the specimen surface are better revealed at +0.5V than at 0V. These dislocations are also etched quite nicely in Fig. 5b. They are shorter, however, because in this case only ~0.4 μm of Si has been removed as compared to ~2.1 μm at 0V and ~1.4 μm at +0.5V. The sensitivity of the preferential etching, *i.e.*, the ratio between the etch-pit size and the amount of silicon which was dissolved, decreases with increasing voltage. At a voltage of

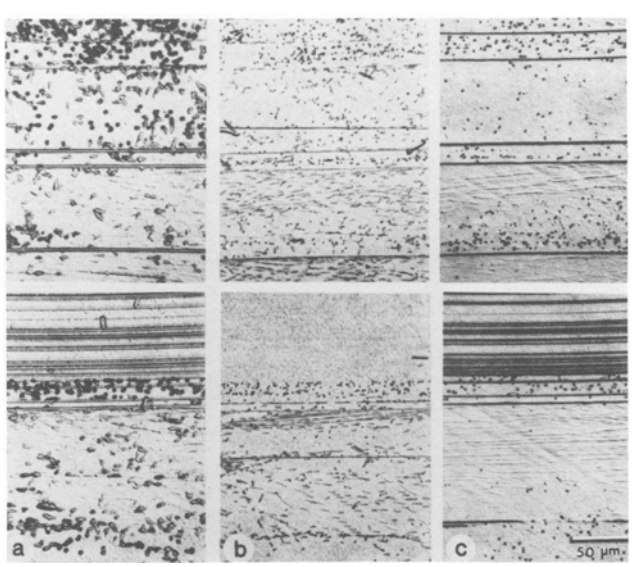

Fig. 5. Anodically etched Si-ribbon at (a) +0.5V, (b) 0V, and (c) −0.4V.

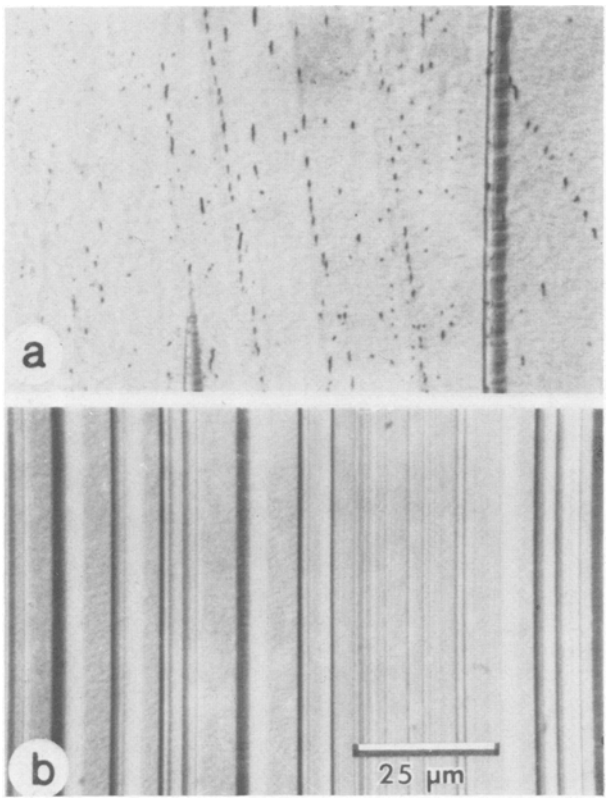

Fig. 6. Si ribbon etched at 5V. In (a) dislocation etch pits are still visible whereas in a neighboring area dislocations are no longer revealed.

5V only steps at grain boundaries are left. Figure 6a shows an intermediate case: pronounced steps have been formed at the boundaries but dislocations are only revealed as very small pits. In neighboring grains dislocations are no longer etched at all, showing that the changeover is somewhat orientation dependent (Fig. 6b).

Geometrically shaped etch pits [as found, *e.g.*, with Sirtl (1) or Wright (3) etch] have never been observed, indicating that etching occurs on all crystallographic planes with comparable etching rates.

Comparison with chemical etching and EBIC.—Figure 7 shows the same area of a poly-Si sample anodically etched at −0.4V (Fig. 7a), +0.4V (Fig. 7b), and with Sirtl etch (Fig. 7c). Although more spectacular examples could have been chosen, these pictures demonstrate several points: (*i*) Sirtl etch did not attack all the twin boundaries present, whereas anodic etching does. (*ii*) Although the etch-pit patterns for dislocations seem to correlate fairly well between Fig. 7a-c (allowing for unavoidable changes in the distribution because several microns of the surface had to be removed between successive etching steps) there are differences: Fig. 7a shows that dislocations are present in the outermost twin boundary which are missing in Fig. 7b and which are only poorly resolved in Fig. 7c. This may indicate that the etching properties of dislocations depend on their type. (*iii*) In Fig. 7a the colored layer has not been completely removed; it can be seen that it does not interfere with the observation of the etching pattern. (*iv*) The EBIC picture of the same area (Fig. 7d) corresponds better to Fig. 7a than to Fig. 7b and c.

Similar behavior can be observed for Si ribbons. Figure 8 shows a Sirtl-etched area next to an anodically etched one. With one exception the twin boundaries are not visible in the anodically etched part of the sample.

Secco-etched samples may show a better correlation to anodically etched ones because dislocations on all crystal planes are revealed. With respect to boundaries it appears to work similar to Sirtl etch. Interestingly, Secco etch applied to ribbons sometimes left a rough surface full of small pits very similar to the rough surface sometimes obtained with anodic etching.

It has been shown that twin boundaries, especially coherent twin boundaries in Si ribbons, often do not significantly influence the electronic properties of the crystal, *e.g.*, the carrier collection efficiency of a solar cell (19). Because twin boundaries can be made to disappear completely in anodic etching there seems to be a correlation between their electrical activity in solar cells and their anodic etching behavior. Both ribbon and poly-Si samples were therefore subjected to a test of the electrical activity of their defects using a scanning microscope in the EBIC mode. Figures 9 and 10 show some results, another example was already given in Fig. 7. The correspondence between the EBIC pictures and the anodic etching pictures is one-to-one for a negative bias voltage of the sample. This has been observed in many more cases than can be shown here. It is particularly interesting that the few twin boundaries out of a whole bundle which show electrical activity in EBIC are also revealed in the anodic etching whereas the electrically inactive twin boundaries appear only at higher etching voltages. Figures 9 and 10 show that the etch pattern is much clearer than the EBIC picture thus allowing a more detailed interpretation of the electrically active defects.

Discussion

Enhanced dissolution rate of defects.—The dissolution rate of a given area of Si is proportional to the current passing through it, *i.e.*, the current density.

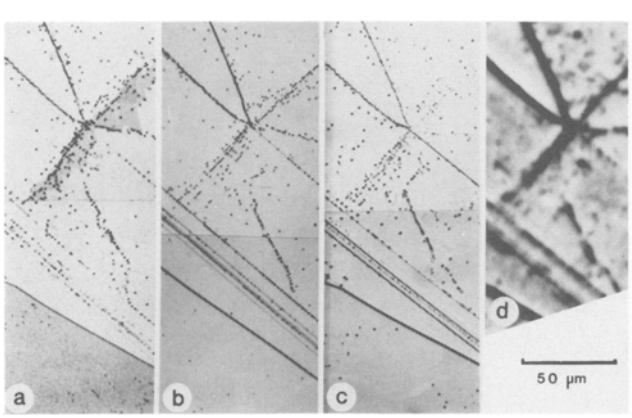

Fig. 7. Comparison between anodic etching, Sirtl etching, and EBIC in poly-Si. For details see text.

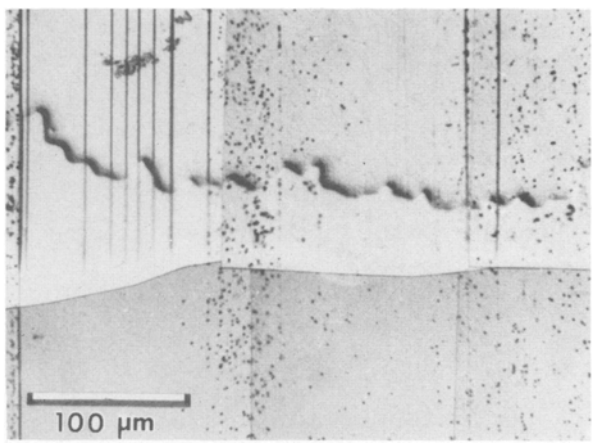

Fig. 8. Comparison between anodic etching and Sirtl etching in ribbon Si.

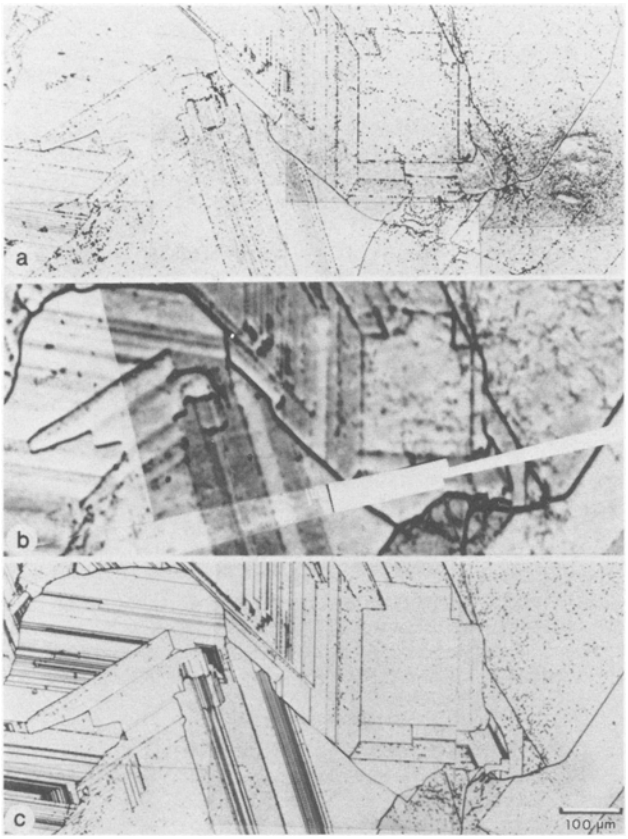

Fig. 9. Poly-Si etched anodically at —0.4V (a) and with Sirtl etch (c). Figure 9(b) shows the EBIC image of this area.

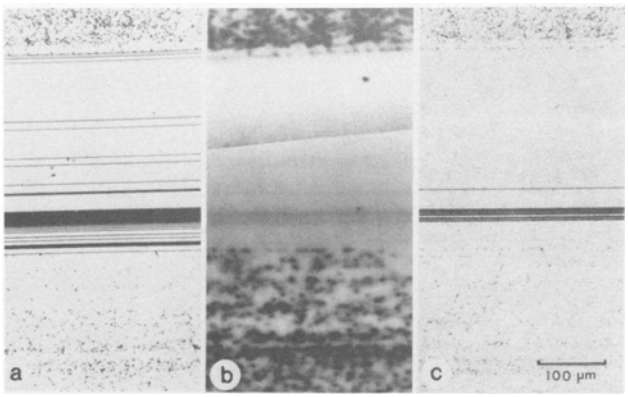

Fig. 10. Comparison between anodic etching at +0.5V (a), EBIC (b), and anodic etching at —0.4V (c) in ribbon-Si.

Preferential etching of defects thus requires higher current densities at the intersection of defect and surface as compared to the undisturbed surface. The current density at a given voltage depends on several factors; the most important ones are the resistance of the electrolyte, the generation and transfer of charge at the silicon-electrolyte interface, and the bulk properties of the silicon.

At high voltages the current density is limited by the resistance of the electrolyte only and practically does not depend on any specific interface or bulk properties of the silicon. The current density across the interface is governed by the HF concentration, thus electropolishing will occur.

At intermediate voltage ranges pronouncedly different etching rates are observed for different surface orientations. This demonstrates that surface properties are dominating the current density in this voltage region. This is in general agreement with the observation that the holes required for the dissolution process are generated in the near-surface regions rather than in the bulk of the Si (9). This is in contrast to Ge where holes from the bulk are diffusing to the interface. The concentration of holes generated near the surface is related to the bulk concentration and their flow across the interface is not inhibited since the band-bending introduced by the applied voltage favors the flow of current.

At very low or negative applied voltages the bulk concentration of holes (and the surface concentration related to it) is no longer important. This is demonstrated by the fact that the potential current curves for p- and n-type Si are almost identical for small applied voltages, *i.e.*, for small overpotentials (15). The current density for n-type Si of low overpotentials can be even higher than that of p-type Si (15), indicating a possible surface inversion-layer. Thus it appears that not the availability of holes but their transport across the interface is rate determining. In other words, potential barriers between hole states in the semiconductor and in the electrolyte may exist, making current flow difficult. Defects may introduce additional transition possibilities for holes to the electrolyte.

A full understanding of the current-potential curves of semiconductors with and without defects requires a sophisticated theory which is beyond the scope of this paper. Phenomenologically, the difference in etching rates for defects and for perfect material can be described by appropriately chosen voltage-current characteristics. From the limited number of experiments performed so far a rough idea of these characteristics can be derived; this is shown in Fig. 11. Comparing these curves to characteristics given in (15), it is clear that defected areas in p-type Si behave as p^+-type Si. In other words, defects in p-type Si behave like p^+-type material; this is in accordance with the general view of the electronic properties of defects in Si, cf. various papers given in Ref. (20).

Dislocations and grain boundaries other than twin related boundaries appear to be etched under most conditions although they may show some voltage dependence as illustrated in Fig. 7. Thus they are strongly electronically active and this is related to the states in the bandgap introduced by them (20, 21). Most twin boundaries, on the other hand, are not etched at small negative voltages. This may indicate that no electronic states in the bandgap are associated with them. However, the fact that they are preferen-

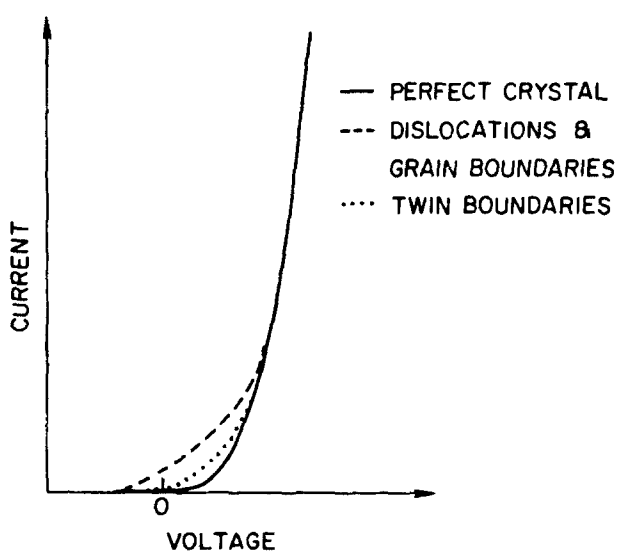

Fig. 11. Tentative current-voltage curves for various defects

tially etched at small positive voltages [scanning electron microscopy showed that true etch grooves and not steps were formed (Fig. 12)] indicates that they do influence the electronic structure of the semiconductor to some extent. This might be due to a change in the surface states around the twin boundaries rather than to states in the bandgap. It may also explain why chemical etching usually does attack twin boundaries and stacking faults (which are closely related defects) although these defects do not have an appreciable strain field or electrical (bulk) activity and cannot always be assumed to be decorated with impurities.

The correspondence between EBIC and anodic etching at negative voltages is striking, even for fine details. This indicates that anodic etching essentially probes the same properties of the defects as EBIC does, namely their ability to act as carrier recombination or generation centers. Of particular interest here is the observation that certain twin boundaries may be electronically active while others are not. This was attributed to the presence of dislocations in these boundaries (17) but this could not be confirmed in the present work.

Chemically etched specimens looked similar to specimens etched anodically at a certain voltage. It appears that Secco etch corresponds roughly to anodic etching at ~0-1V and Sirtl etch to somewhat higher voltages. Since chemical etching is also an electrochemical reaction, the present experiments may lead to a better understanding of their operation.

Some remarks on the applicability of the method.— Anodic etching offers a simple and elegant way to obtain defect information about defects in Si which usually would require EBIC and chemical etching. It has considerable advantages compared to EBIC, the setup and the preparation is simple as compared to the rather complex specimen preparation and equipment needed for EBIC. The resolution is much better for anodic etching and large areas can be etched and inspected in a short time. On the other hand, EBIC is nondestructive and can be made quantitative whereas anodic etching requires the dissolution of a thin surface layer (≤ 1 μm) and is as yet not quantitative.

Anodic etching can replace chemical etching if the correct voltage is chosen. The sensitivity seems to be better than that of most chemical etches and there is no ambiguity about the selectivity of the etching with respect to certain surface orientations or certain defects.

It is important to note that the method is not restricted to p-type Si; n-type Si can be anodically etched in much the same way as was already demonstrated in Ref. (14). Moreover, the method very likely can be applied to any semiconductor if a suitable electrolyte can be found. This might be difficult, but certainly it is less so than the development of a chemical etch.

It is felt that the method could be made quantitative if a better theoretical understanding of the basic process could be achieved and if quantitative experimental results could be supplied. The latter would involve precise measurements of the Si-potential-current relationship rather than simple voltage-current characteristics and should also define the role of the resistivity of the Si.

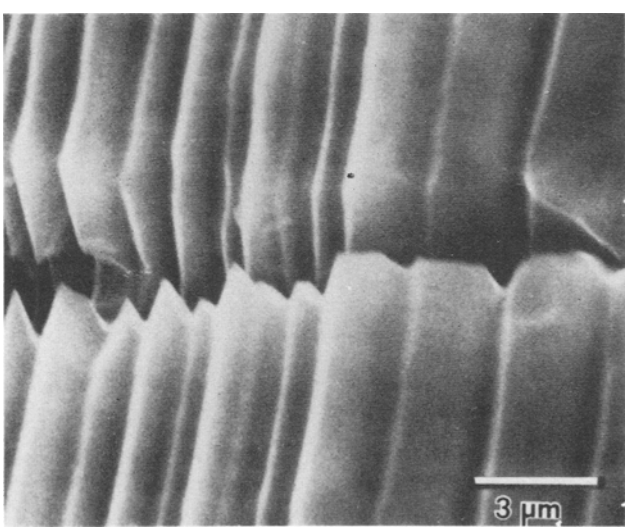

Fig. 12. SEM picture of etch-grooves at twin boundaries crossing a scratch-mark in ribbon Si after anodic etching at +0.5V.

Conclusions

1. Defects in p-type Si can be etched anodically and their etching behavior depends on the applied voltage.
2. At very low potentials only defects are etched which would be classified as "electrically active" by EBIC.
3. At somewhat higher potentials the etching is similar to chemical etching but is more sensitive and free of ambiguities.
4. Anodic etching has the potential to develop into a powerful technique for defect characterization in many semiconductors for both p- and n-type and can widely replace EBIC and chemical etching.

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Applications of a Low Noise Potentiostat in Electrochemical Measurements

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ABSTRACT

Measurements on two electrochemical systems, copper in copper sulfate and aluminum in boric acid/tetraborate buffer, have been carried out by recording the amplitude spectrum of the fluctuations in the current density. For these measurements, a low noise potentiostat developed and built at NBS was employed. In the case of copper, the current spectra are found to be the deterministic response of the electrode to the noise voltage generated by the potentiostat. The electrode characteristics for charge-transfer and for diffusion could be obtained from the impedance plots derived from the measurements when the level of the applied signal was of the order of 10^{-7}V. In the case of aluminum, the deterministic response observed in the absence of pitting gave way to random fluctuations in the current in conditions leading to pitting. It is shown that the onset of pit formation can be detected from noise measurements. The significance of the information obtained in electrochemical noise measurements is briefly discussed.

The study of random fluctuations in current and potential of electrodes, usually known as electrochemical noise, is receiving increasing attention, and interesting applications are being envisaged in the field of corrosion (1). In these studies, it is often necessary to detect and measure very low amplitude signals, and it is therefore very important to reduce the noise generated by the measuring instruments. Since in most electrochemical studies it is desirable to control the electrode potential, a low noise potentiostat is a particularly useful device (2).

Elsewhere (3), the circuit and performance of a potentiostat designed and built at NBS have been described. The purpose of this communication is to report on measurements carried out on some electrochemical cells, taking advantage of the characteristics of such a potentiostat. These measurements are not restricted to the detection of noise, but concern also the observation of the current response to very small voltage signals.

Experimental Procedures

The measurements were carried out with the apparatus shown schematically in Fig. 1. All the instruments inside the dot-dashed enclosure are battery operated, and the enclosure represents electromagnetic shielding as well as some protection from mechanical vibrations. The potentiostat provides for a low noise d-c control voltage and for the measurement of the d-c current. A built-in a-c amplifier is employed for the detection of the fluctuations in the current in the frequency range approximately between 0.1 Hz and 2 kHz. The cell is provided with two reference electrodes, a low impedance one, which is used as a sensor for the potentiostat and for the measurement of the voltage noise, and a second one, often an SCE, employed for the monitoring of the d-c electrode potential. The values of the d-c voltage and current are recorded on a two-channel recorder.

An additional voltage signal can be added to the d-c control voltage. In this work, the superimposed voltage consisted of a constant amplitude, swept frequency signal, sweeping linearly over a factor of ten. The repetition rate was slightly less than the time of acquisition of a spectrum by the spectrum analyzer.

The frequency analysis of the output signal, either the current or the electrode potential, depending on the position of the switch shown in Fig. 1, was carried out by a spectrum analyzer with a frequency resolution of 1/200 of the range. In the 50 Hz range, for example, the spectrum consisted of 200 values at intervals of 0.25 Hz. The acquisition time for one spectrum is equal to one period at the lowest frequency, that is, 4 sec for the range mentioned above.

The input waveform to the spectrum analyzer as well as the instantaneous and average spectra were observed continuously on the oscilloscope. Average spectra were then recorded on an X-Y recorder, either on a linear or on a logarithmic scale.

The time involved in acquiring the average spectra in the low frequency ranges can be considerable. In the 5 Hz range each spectrum requires 40 sec so that for an average over 64 spectra the acquisition time is of the order of 40 min.

Experimental Results

The results presented here concern two quite different electrode systems, one having low and the other high resistance to the faradaic current. As a low impedance system, the reaction between Cu metal and a 0.5 mole/liter $CuSO_4$ + 0.1 mole/liter H_2SO_4 solution was examined. Figure 2 and 3 show the voltage and current spectra, respectively. The reference electrode was also copper, and the data were taken in conditions of zero d-c current. The spectra were also taken when a swept frequency signal was added to the d-c control voltage. The amplitude of the signal as shown in Fig. 2 was about 10-100 times the background noise but never larger than about 2 μV. Figure 3 shows the current response with and without the superimposed voltage signal.

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Key words: aluminum, copper, impedance measurements, pitting, potentiostat.