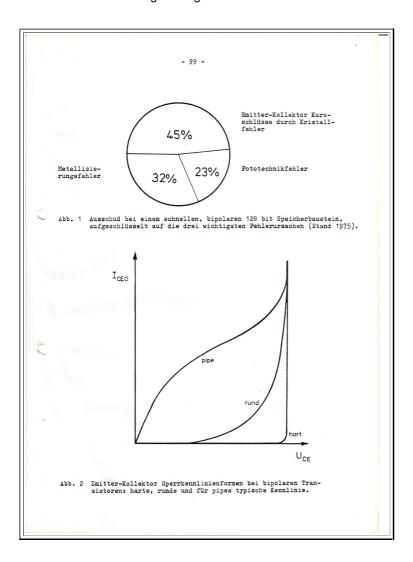
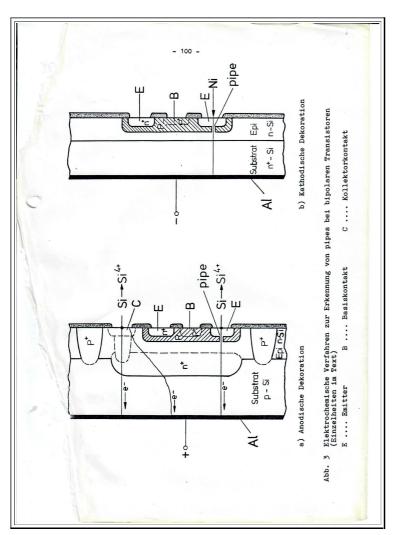
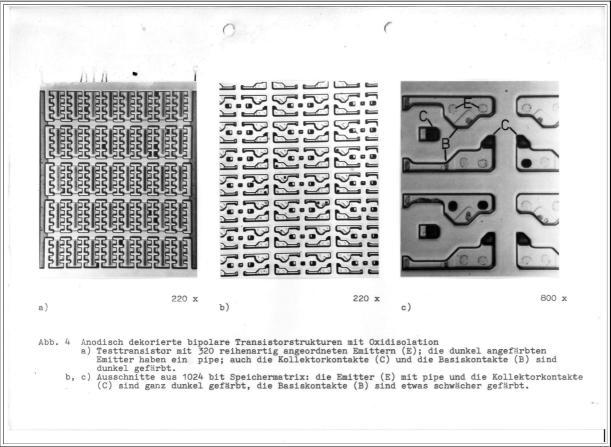
## Pictures to: Kristallfehler in hochintegrierten Schaltkreisen aus Silizium Part 1

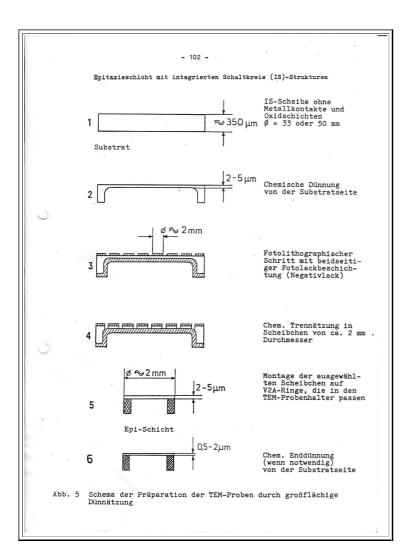
## (Crystal Lattice Defects in Highly Integrated Silicon Devices)

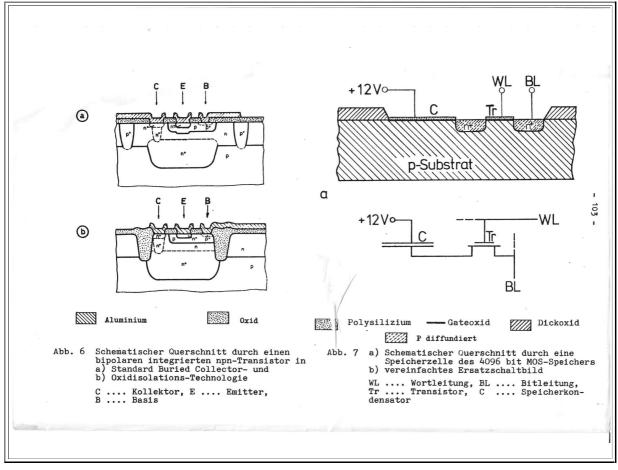
- In what follows you see the second part of the "Abbildungen" (Pictures) as they occur in the report. The scans were made from my still existing copy and some of the pictures were somewhat processed by me to improve clarity.
  - The figure captions are included so there is no need for further text.
     Here we have Fig. 1 Fig. 21

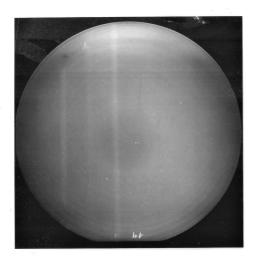


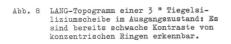












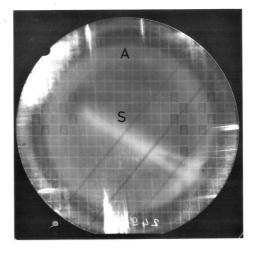
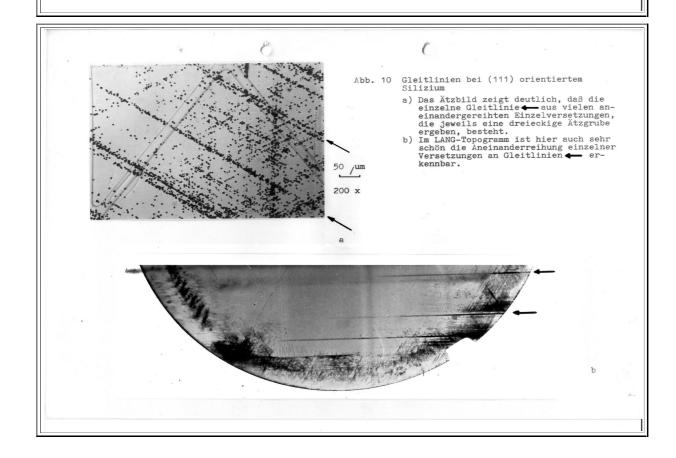
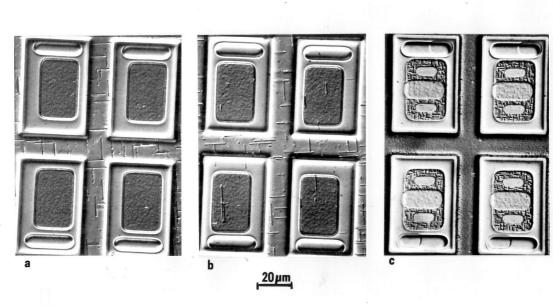


Abb. 9 LANG-Topogramm einer 2 " Scheibe mit fertigen bipolaren Speichersystemen in ASEC-Technologie, die Gleitbereiche am Rand, einen Schleier S und ringförmige Sauerstoffausscheidungen A aufweist. (Die drei schräg verlaufenden gwauen Streifen sind apparaturbedingt.)

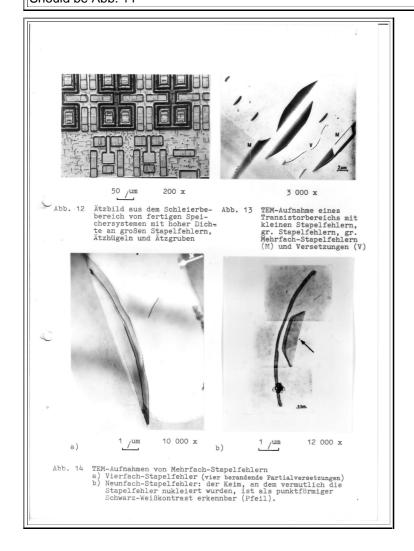


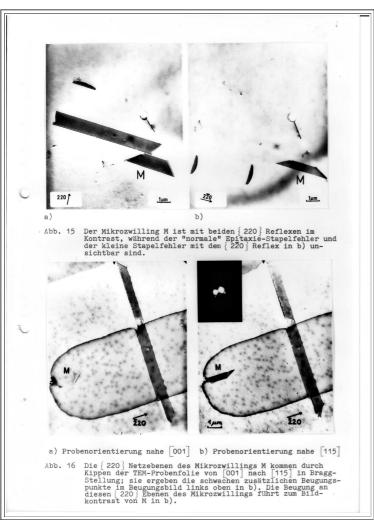


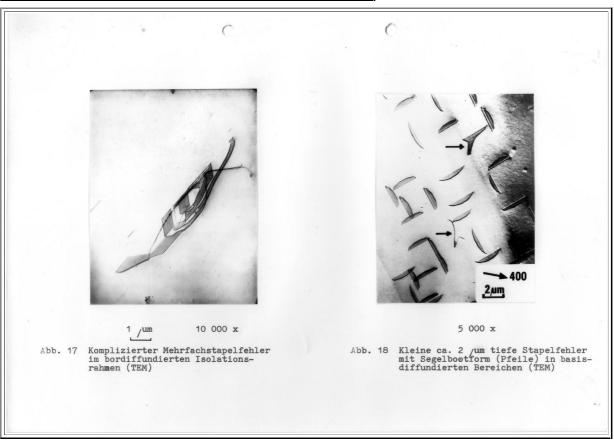
- Abb. (Große Stapelfehler, kleine Stapelfehler und Versetzungen im Ätzbild (30 sec Ätzzeit)

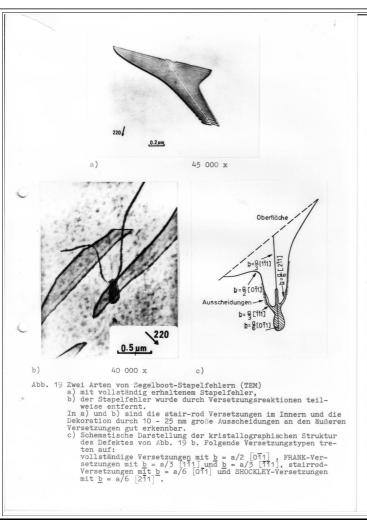
  - a) große SF nur außerhalb der Transistorfelder (im Isolationsdiffusionsbereich) b) große SF innerhalb (geringe Dichte) und außerhalb (höhere Dichte) der Transistorfelder; Atzungen bei a) und b) an Scheibe nach Basisdiffusion; auch Ätzgruben von Versetzungen sind zu seh
  - c) kleine-SF im basisdiffundierten Bereich von Transistoren; Ätzbild von fertiger Scheibe

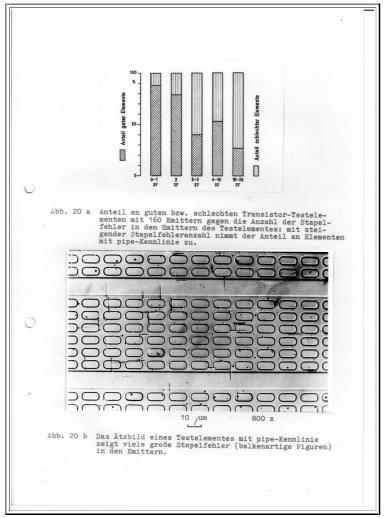
## Should be Abb. 11

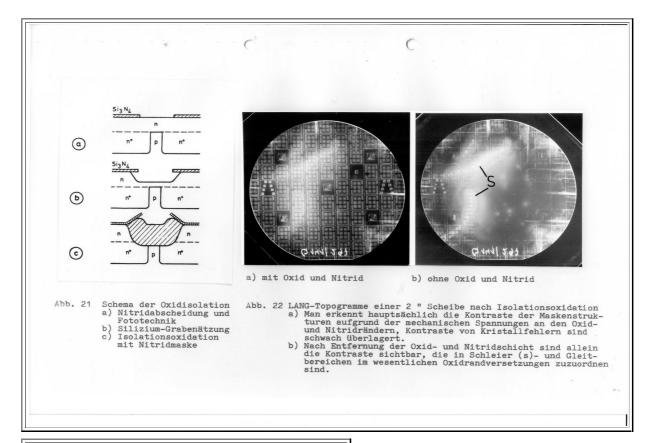












Continue with Fig. 23 - 45