Proceedings of the Third International Symposium on
Silicon Materials Science and Technology

(11)

H. Fod
proc.1977

SEMICONDUCTOR SILICON 1977

Edited by

Howard R. Huff
Texas Instruments Incorporated
Houston, Texas

Erhard Sirtl
Wacker-Chemitronic
Burghausen, West Germany

Assistant Editors

K. Benson
J. Bloem
W. M. Bullis
H. Herzer
C. M. Osburn
K. Pickar
K. V. Ravi
G. A. Rozgonyi
Y. Takeishi
F. G. Vieweg-Gutberlet
P. Wang
J. Zoutendyk

ELECTRONICS AND ELECTROTHERMICS AND METALLURGY DIVISIONS

Proceedings Volume 77-2

THE ELECTROCHEMICAL SOCIETY, INC., P.O. Box 2071, Princeton, N.J. 08540

ADVANTAGES IN THE STUDY OF CRYSTAL DEFECTS IN SILICON DEVICES BY USE OF A HIGH-VOLTAGE ELECTRON MICROSCOPE (HVEM)

H. Föll[1] and B.O. Kolbesen[2]

[1] Max-Planck-Institut für Metallforschung, Institut für Physik, D-7000 Stuttgart 80, Büsnauerstraße 171, Fed. Rep. Germany

[2] Siemens AG, Grundlagenentwicklung Halbleiter, D-8000 München 46 P.O.Box 460705, Fed. Rep. Germany

HVEM combined with a large area specimen thinning technique, compared to conventional 100 kV electron microscopy, offers several advantages, e.g., electron transparent areas ≥ 1 mm^2 and increased thickness of samples (2 µm - 5 µm). By this technique process-induced defects (dislocations, stacking faults, precipitates) in bipolar and MOS devices were studied. A strong correlation between several species of defects and device failure modes was found. A special type of diffusion-induced stacking fault could be shown to cause emitter-collector shorts in bipolar devices with shallow pn-junctions. Large oxidation-induced stacking faults are often very complicated with respect to their crystallographic structure and were frequently identified to be rather microtwins than stacking faults.

1. INTRODUCTION

It is nowadays well established that crystal defects can be detrimental to silicon semiconductor devices (see, e.g., the review articles /1,2/). A large number of diagnostic methods exist (e.g., chemical etching, X-ray and IR-topography, scanning electron microscopy in special modes and transmission electron microscopy (TEM)) which can be used to investigate crystal defects in starting material and in devices. Each of these methods offers advantages and disadvantages. Optimum information can be obtained if several methods are applied in conjunction with each other.

It is the aim of this paper to demonstrate that, in particular, high-voltage electron microscopy (HVEM) combined with an appropriate specimen preparation technique is a powerful tool, often irreplaceable by other methods, for the study of the microscopic nature of crystal defects. It is especially suitable to establish one-to-one correlations between specific defects and certain failure modes of silicon devices. In the following we will briefly describe important aspects of the method and give some selected examples of crystal defects which caused catastrophic failures in devices. In some of these examples HVEM was practically the only method which was able to identify the true nature of these defects.

2. EXPERIMENTAL

Conventional transmission electron microscopy (CTEM) performed at beam voltages around 100 kV, has been used for about 15 years to study defects in silicon starting material and processed wafers. The restriction to silicon foils of a thickness of $\leq 1\,\mu m$ is a serious disadvantage. Normally such thin foils contain only a fraction of the electrically active layer of the device of interest. Especially the pn-junctions are no longer contained in those foils. Furthermore, the preparation of such thin foils is cumbersome, especially with the common techniques /3,4/.

Most of these difficulties and restrictions can be overcome by HVEM combined with the 'large area thinning procedure' /5/ for the specimen preparation. Depending on the actual beam voltage of the HVEM and the resolution demanded, silicon foils with a thickness of $4-8\,\mu m$ are investigable. In the case of large-scale integrated circuits $2-5\,\mu m$ thick specimens frequently contain the whole electrically active layer (i.e. the epitaxial film) and may be investigated without difficulties.

For the investigation of MOS devices it is often important to prepare specimens which include the oxide layer or at least parts of it (e.g., the 100 nm thick gate oxide). Without this oxide layer valuable information about defects at the $Si-SiO_2$ interface cannot be obtained. An amorphous oxide layer on a silicon specimen otherwise strongly reduces its transparency to the electron beam because of its diffuse scattering of the electrons. For the investigation of such specimens a HVEM is therefore often an imperative requirement.

'Thick' HVEM specimens can easily and quickly be prepared compared to corresponding CTEM samples. The application of the large area thinning procedure /5/ permits a simple and precise area selection of a large number of HVEM specimens simultaneously from one wafer. The area of the specimen which is transparent to the electron beam is only limited by the goniometer geometry of the HVEM (in our case the inner diameter of the specimens was generally about 1 mm).

In our investigation of crystal defects in silicon devices we have used chemical etching (Sirtl etch) and X-ray topography besides HVEM. The results of these three methods were compared to findings previously obtained by electrical measurements at test patterns which were representative for the function and the properties of the devices of interest. The main aim was to establish one-to-one correlations between devices failures, e.g., emitter-collector shorts ('pipes' /6/) in bipolar transistors with shallow pn-junctions and crystal defects. For this purpose test transistors with a single emitter (emitter area $5 \times 10\,\mu m^2$) were used normally. These 'single' transistors were contained in every chip of a normal device or in special test chips of the wafer. Principally 'good' and 'bad' test devices have been investigated in the HVEM in order to be sure of the significance of the results. Up to now the number of pn-junctions investigated (or $Si-SiO_2$ interfaces, respectively) exceeds some thousand.

3. RESULTS

Although the crystal defects found in the processed wafers are often of complicated nature and cannot be described properly in the usual terms of 'stacking faults' or 'dislocations', for the sake of simplicity, we may classify them into four groups and discuss their influence on electrical parameters of devices separately. These groups are i) dislocations, ii) stacking faults, iii) precipitates and iv) substrate defects.

3.1 Dislocations

'Glide dislocations' frequently are introduced during the epitaxy process or during the heating or cooling period of high-temperature processes. It is well known that glide dislocations can cause pipes in bipolar transistors /7,8/. We have obtained almost a one-to-one correlation between these dislocations and piped 'single' transistors. In no case was a decoration of the dislocations causing a pipe observed. In MOS devices with oxide layer the traces of glided dislocations are visible as broad dark lines, indicating that marked stresses are present at the $Si-SiO_2$ interface. These glide traces annealed during the electron bombardment within a few minutes and became invisible. It seems that in devices containing a large number of these glide traces the minority carrier lifetime is decreased, but there is no strong correlation.

'Oxide-edge dislocations' are often observed in bipolar transistors which are electrically isolated by oxide wells produced in a localized oxidation process /9,10/. Fig.1 shows a 'single' transistor with a dense dislocation array. The dislocations also penetrate the emitter area, their density locally can amount up to 10^9 cm^{-2}. It is supposed /11/ that stresses introduced by the volume expansion of the oxide are responsible for the generation of these dislocations. Between these dislocations and pipes (or soft breakdowns) of single transistors, apart from a few exceptions, a one-to-one correlation was found. The investigation of these devices supplies a typical example for the superior possibilities of HVEM. It is practically impossible to prepare such specimens for CTEM because between the transistors and the surrounding areas typically a thickness step of about 2 µm in the silicon occurs.

'Dislocation clusters', generated by mechanical damage, e.g., indentations of tweezers, scratches etc., were sometimes observed in test devices of both bipolar and MOS wafers. Dislocation clusters penetrating the pn-junctions of bipolar transistors (Fig.2a) caused catastrophic pipes, in the case of MOS capacitors (Fig.2b) an enormous decrease in the minority carrier lifetime was ascertained.

Finally, it should be noted that further 'kinds' of dislocations (e.g., misfit dislocations, dislocations resulting from: stacking fault reactions, prismatic loop punching, point defect condensation etc.) are observed frequently. They are generally found to be of detrimental influence on electrical device parameters.

3.2 Stacking faults

'Large stacking faults' (SF) (5 – 50 µm in length, 1.5 – 3 µm in depth, extrinsic nature) are often formed during epitaxial growth and/or high-temperature processes in oxidizing environment and dealt with in numerous papers (see, e.g., /12-16/). In heavily diffused areas sometimes even SF networks, similar to misfit dislocation networks, are observed (Fig.3a). These SF occur frequently as multiple SF's, i.e., many stacking faults overlap closely and have often exactly the same shape. Fig.3b shows a SF which is at least nine-fold. These multi-stacking-faults may equally well be described as microtwins. In fact, a remarkable fraction of the SF's shows a strong contrast, if imaged with a {220} diffraction vector at which normal stacking faults are not in contrast, provided the foil normal is titled exactly in the {115} position. Then the {111} planes of the microtwins are in Bragg position, the fault appears in a strong dark contrast. Fig.4 shows an example of a large SF, small SF's and a microtwin. It is well known that these SF can cause pipes /6,7/. We have found an unambiguous statistical correlation between the number of SF in a multi-emitter transistor and the number of piped transistors. It is felt that the electrical differences of SF are correlated to their differences in structure. Multi SF or microtwins, respectively, seem to be of more detrimental influence than normal SF.

Small stacking faults (~ 2 µm in length, ~ 0.4 µm in depth, extrinsic nature) were found frequently in special bipolar integrated circuits (Fig.5). They are generated during base diffusion processes. In the presence of large SF's they occur only in a strongly reduced concentration. Within about 100 of these small SF's generally one species of special shape was observed which often resembles the body of a sailing boat (Fig.6). These 'sailing-boat' stacking faults which are also generated during the base diffusion process very often change their structure by a shearing process during the subsequent emitter diffusion processes (Fig.7a). Parts of the fault were removed and perfect dislocations were formed. The dislocations of the fault are often decorated, presumably with small precipitates of impurities of about 10 – 25 nm in size). The penetration depth of these 'sailing boat' can be 2 µm or even more (thus such a defect can be studied only by HVEM). Transistors which contained a SF in the emitter area are invariably piped. The crystallographic structure of these defects is somewhat complicated and given schematically in Fig.7b. They originate from the interaction of two small SF's which are generated by the same nuclei on neighbouring {111} lattice planes.

In MOS capacitors sometimes a strange species of defects was found which originates from large stacking faults. Two modifications of these defects were observed. The first one originates from an unfaulting of a large SF, the resulting perfect dislocation loop and now also the intersection of the stacking fault primarily present at the $Si-SiO_2$ interface can be seen (Fig.8, defect 'D'). The second modification (Fig.8, defect 'I') is completely located at the $Si-SiO_2$ interface as has been ascertained by stereo microscopy. This fault develops from the

first one by a glide process of the perfect dislocation to the interface driven by image forces. All parts of the two modifications which were located at the interface vanished during observation within a few minutes due to radiation damage in the SiO_2 layer (Fig.8b). In MOS capacitors these defects cause a distinct decrease of the minority carrier lifetime.

To summarize, it should be emphasized that the simple 'stacking fault' as observed by etching techniques or in parts by X-ray topography or even by CTEM is practically not existent. In silicon devices the 'stacking faults' are mostly of a highly complex structure and quite different. Thus their different behaviour with respect to electrical properties of the device is not amazing. In the following we shall use the term 'stacking fault' in a general sense to denote all types of planar defects.

3.3 Precipitates

Generally, precipitates or a decoration of defects was observed rather seldom. In heavily diffused device regions sometimes small precipitates (10 – 50 nm in size) are found, presumably formed by the dopant atoms. These precipitates, since normally not present in the pn-junctions, have no influence on electrical parameters of the device.

Of more interest are precipitates in connection with stacking faults. Apart from the small precipitates in connection with the 'sailing boat' SF already mentioned (and which, as should be borne in mind, may also be small dislocation loops as in the case of swirl defects, cf. /17/) in some specimens all intermediate stages between stacking faults and precipitates are found. In the first step precipitates are attached to the partial dislocations of the stacking fault. Using dynamical imaging conditions, they appeared in a 'tree-ring' contrast (Fig.9a). It could be shown by contrast experiments and stereo micrographs that these precipitates are rather planar, with a displacement vector perpendicular to their plane. Thus the fringes cannot be due to thickness variations, their origin is not understood so far. High resolution weak beam micrographs (Fig.9b) show that these precipitates are composed of a large number of very small agglomerates (diameter 10 nm). At a later stage, the precipitation occurs also in the plane of the stacking faults, misfit dislocations may be generated and a complex structure is observed. In connection with the small SF (except 'sailing boat' SF) precipitates are of no bad influence. Precipitates coupled with large SF's were never observed in pn-junctions.

In contrast, the normal stacking faults appeared to be decoration-free. Using {113} reflections, no residual contrast, which might indicate a decoration (cf. /18/), was observed.

3.4 Substrate defects

In the substrate material often regions with defects of different density and different structure could be distinguished in processed wafers by X-ray topography and by etching. These differences of the defect structure in the substrate are reflected by differences of the

defect structure in the epitaxial layer, e.g., occurrence of oxide-edge dislocations, or of large or small stacking faults. HVEM investigations of the substrate material after several high-temperature processes yielded the following result: The typical substrate defects are systems of concentric faulted dislocation loops of extrinsic type which additionally contain concentric circular chains of small dislocation loops (diameter $\leq$ 100 nm) of extrinsic type, too (Fig.10). Only in the centre of the defect a random distribution of the small loops is observed. These defects are similar to the defects observed in Czochralski-grown silicon after one or two annealing processes in /18,19/, but are much more complex due to the larger number of different high-temperature processes. Moreover, the defects observed in our specimens did not show distinct precipitation effects.

The differences between the defects from regions looking different in the X-ray topographs or etch patterns are the following:
In regions with a higher defect density the defects exhibit a lower degree of complexity in the HVEM (Fig.10a), in regions which contain a lower concentration of defects the defect structure is of a higher complexity (Fig.10b).
Other defects like small precipitates or dislocations and dislocation clusters (cf. Fig.10b) are also observed in the substrate material. These are well-known /18,19/ and were not extensively studied in our work.

ACKNOWLEDGEMENTS

The authors are indebted to Drs. K. Mayer, H. Murrmann, H. Strack, H. Strunk and M. Wilkens for their contribution to the experimental work and for valuable discussions. They are grateful to Miss L. Holl and Mrs. E. Kutschera for performing the photographic work and to Mrs. C. Bergmann for her excellent and kind assistance during the preparation of the manuscript. The competent technical assistance of G. Schuh who prepared the specimens is especially acknowledged.

REFERENCES

/1/ G.H. Schwuttke, Microelectron and Rel. 9, 397 (1970)

/2/ J.E. Lawrence, "Semiconductor Silicon-1973", H.R. Huff and R. Burgess, Eds., the Electrochem Soc. Softbound Symposium Series (1973), 17

/3/ G.R. Booker, R. Stickler, Brit. J. Appl. Phys. 13, 446 (1962)

/4/ G. Das, N.A.O'Neil, IBM J. Res. Develop. Jan. 1974, 76

/5/ B.O. Kolbesen, K.R. Mayer, G.E. Schuh, J. Phys. E. (Scientific Instrum.) 8, 197 (1975)

/6/ F. Barson, IEDM (Intern. Electronic Device Metting) 447 (1975)

/7/ F. Barson, M.S. Hess, M.M. Roy, J. Electrochem. Soc. 116, 304 (1969)

/8/ W.K. Tice, R.C. Lange, R.B. Shasteen, "Semiconductor Silicon-1973", H.R. Huff and R. Burgess, Eds., the Electrochem. Soc. Softbound Symposium Series (1973), 651

/9/ J.A. Appels, M.M. Paffen, Philips Res. Repts. 26, 157 (1971)

/10/ E. Kooi, J.G. van Lierop, W.H.C.G. Verkuijlen, R. de Werdt Philips Res. Repts. 26, 166 (1971)

/11/ A.E. Cosand, S. Prussin, Extended Abstracts of the Electrochem. Soc. Meeting, Washington D.C. 1976, 292

/12/ R.H. Finch, H.J. Queisser, G. Thomas, J. Washburn, J. Appl. Phys. 34, 406 (1963)

/13/ S. Prussin, J. Appl. Phys. 43, 2850 (1972)

/14/ C.M. Hsieh, D.M. Maher, J. Appl. Phys. 44, 1302 (1973)

/15/ K.V. Ravi, Phil. Mag. 30, 1081 (1974), 31, 405 (1975)

/16/ S.M. Hu, J. Appl. Phys. 45, 1567 (1974)

/17/ H. Föll, B.O. Kolbesen, Appl. Phys. 8, 319 (1975)

/18/ D.M. Maher, A. Staudinger, J.R. Patel, J. Appl. Phys. 47, 3813 (1976)

/19/ M. Olivier, D. Lafeuille, M. Dupuy, G. Rolland, Extended Abstracts of the Electrochem. Soc. Meeting, Toronto, 1975, 343
M. Olivier, Thesis, Univ. Scientifique et Médicale de Grenoble, 1970

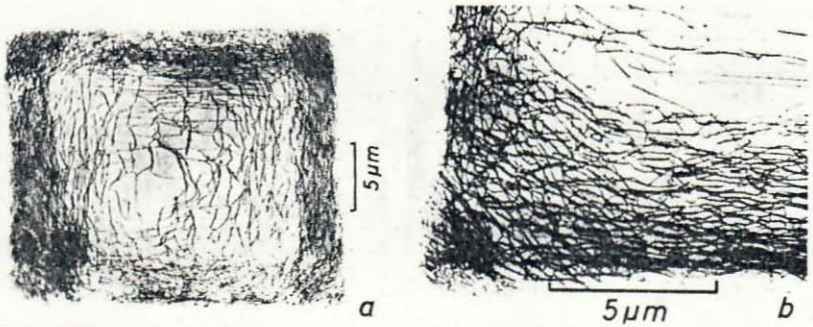

Fig.1 Oxide-edge dislocations in a single transistor. (a) overview, (b) section of the transistor with high dislocation density.

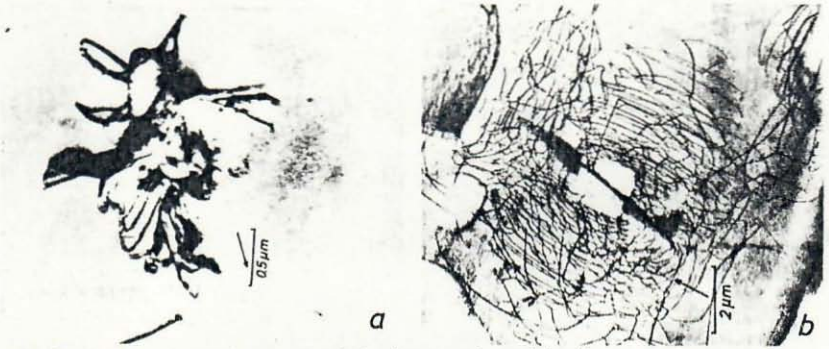

Fig.2 Dislocation clusters. (a) cluster in a bipolar transistor, (b) cluster in a MOS capacitor.

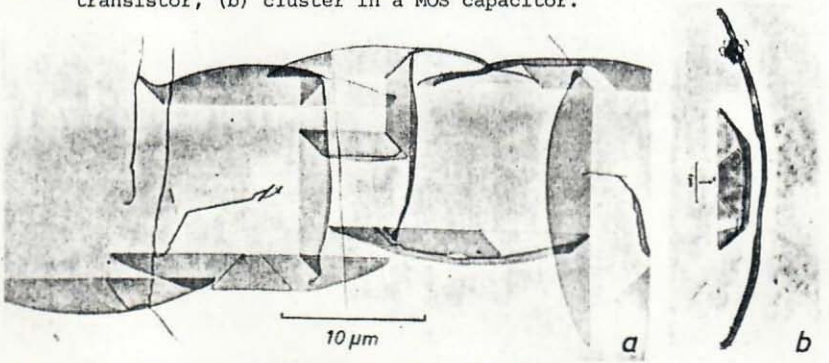

Fig.3 (a) Stacking fault network, (b) nine-fold stacking fault.

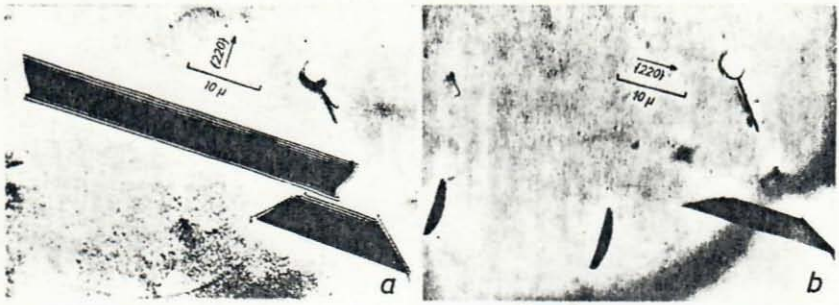

Fig.4 Microtwins, imaged with two different {220} reflexions. The microtwin is always in contrast, the 'normal' stacking faults vanish completely in the appropriate reflexion.

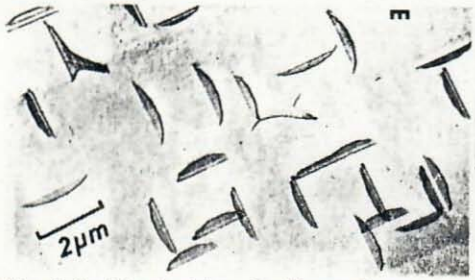

Fig.5 Small stacking faults and a sailing boat stacking fault in the emitter region of a transistor.

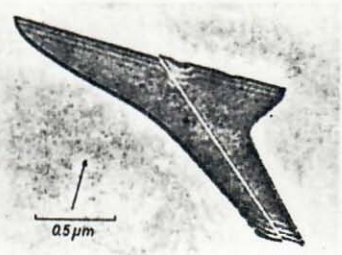

Fig.6 Typical example of an unfaulted sailing boat SF.

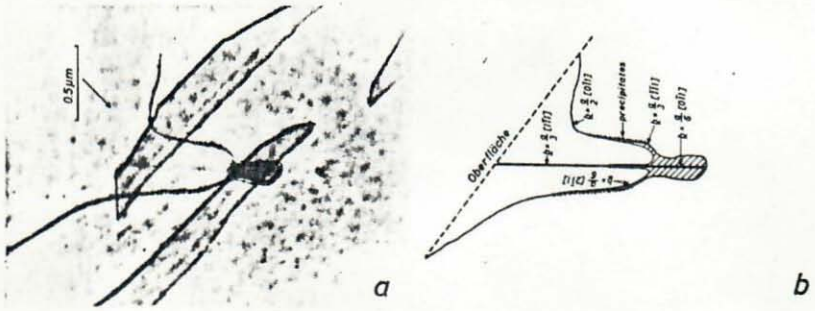

Fig.7 (a) Sailing boat stacking fault after an unfaulting reaction.
(b) Schematical drawing of its crystallographic structure.

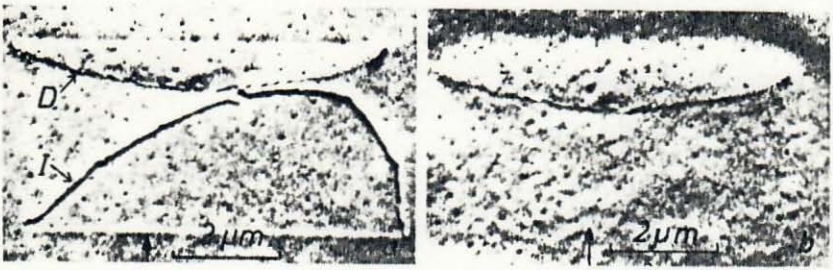

Fig.8 Typical example of MOS defects located at the Si-SiO2 interface. (a) At 'D' a defect resulting from the unfaulting of a large SF, at 'I' a defect completely located at the interface. (b) After some minutes of irradiation the parts of the defects located at the interface have vanished.

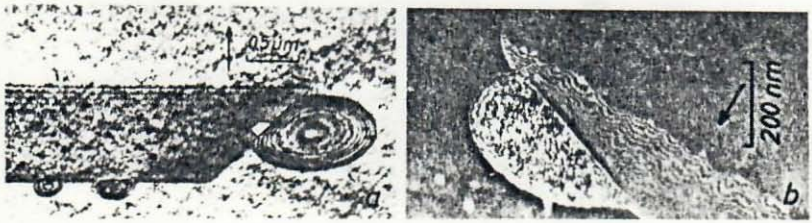

Fig.9 Precipitates correlated with stacking faults. (a) Precipitate showing 'tree ring' contrast, (b) weak beam micrograph demonstrating the fine structure of these precipitates.

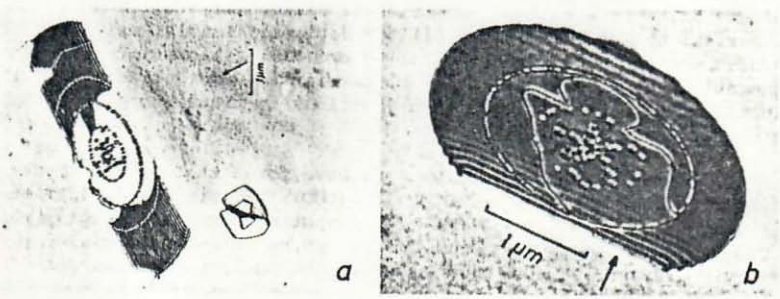

Fig.10 Substrate defects. 1(a) Typical defect in regions of low defect concentration. 1(b) Typical defect in regions with a higher defect concentration.